Optically Powered, Optoelectronic Spatial Light Modulators

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13. ABSTRACT (Maximum 200 words)

We demonstrate a 1.3 μm wavelength optoelectronic hybrid/integrated smart pixel receiver/transmitter circuit. The pixel was fabricated in the InP/InGaAsP material system for compatibility with long-distance fiber optics communication applications. The input and the output signals are optical, while the processing elements remain electronic. The circuit employs monolithically integrated p-i-n photodiodes and heterojunction bipolar transistors (HBT's), along with surface-mounted folded cavity surface emitting lasers (FCSEL).

The circuit has a bandwidth of 100 Mb/s, an input/output gain of 8, and fan-out of 3. The "intelligence" of the circuit lies in its switching, amplification, low power dissipation, and cascadability (the ability to drive several stages in a multi-layer interconnect system). Furthermore, the pixel uses an electrical control to enable or disable the circuit operation. The circuit can be used in a linear or thresholding regime. The sensitivity of the pixel was measured to be -32 dBm at 100 Mb/s as a receiver, giving rise to a switching energy of 14 fJ. With gain and cascadability included, a switching energy of 30 fJ was measured. Both values are the lowest obtained to date for comparable smart pixel technologies.

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The major accomplishments of this successful program have been the following:

- Demonstration of the lowest switching energy integrated optoelectronic smart pixel circuit. Optical switching energies of 30 fJ under "cascadable" conditions (i.e. the input optical on/off contrast is equal to or larger than at the output) is nearly 10 times better than previously achieved using any smart pixel technology.
- Demonstration of a very high efficiency, low threshold current surface emitting laser technology for use at 1.3μm and 1.55 μm wavelengths
- Demonstration of a novel, high gain InGaAs/InP heterojunction bipolar transistor technology suited for very low power dissipation smart pixel applications.
- The first complete, analytical comparison and evaluation of smart pixel technologies based on SEEDs or optoelectronic IC technologies. The comparison looked from both a materials, devices and systems perspective at the fundamental limiting issues to these technologies.
- The first analytical evaluation of smart pixel systems designed specifically to achieve minimum switching energies of <1fJ. This evaluation has considered novel pixel architectures operated at low temperatures and using avalanche photodiodes as the input device.

Details of our results are attached in the body of the report which includes the thesis of a recent graduate student, Dr. Kiandocht Beyzavi. A complete list of publication resulting from research done under the support of this program is also provided in the following pages.

Funds provided by AFOSR have been used to support the following personnel:

Dr. Chih Ping Chao, post-doctoral fellow. Currently at Texas Instruments

Dr. Kiandocht Beyzavi, PhD, 1996

Dr. Guang-Jye Shiau, PhD, 1994. Currently at Applied Materials

Mr. Dong-su Kim, PhD expected 1996.

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ULTRA LOW SWITCHING ENERGY, INTEGRATED OPTOELECTRONIC SMART PIXELS

Kiandokht Beyzavi

A DISSERTATION

PRESENTED TO THE FACULTY

OF PRINCETON UNIVERSITY

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OF DOCTOR OF PHILOSOPHY

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Chapter 1

Introduction

The bandwidth of advanced electronic interconnections is increasingly limited by the propagation delay in the interconnect lines[1]. Several researchers have analyzed and compared the performance of optical and electronic interconnection systems[2,3], concluding that with the current state of technology, for short distances (<1 mm) or low frequencies (<1 GHz), electrical interconnections are superior to their optical counterparts. However, as the distance and the bandwidth increase, large RC time delays limit the maximum achievable bandwidth in electrical interconnections[1].

Furthermore, large circuit layouts typically have significant variations in line length. This results in different parts of the circuit receiving the clock at slightly different times, an effect referred to as clock skew[4]. The other significant bandwidth limitation to electrical interconnections is reactive crosstalk between lines. Crosstalk increases as the chip dimensions decrease and packing density gets larger[5]. With the decrease in chip dimensions, resistance increases as the cross sectional area of metal interconnects is reduced, which further limits the bandwidth[6]. Another limitation in VLSI circuits is the input/output pin-out density (I/O), which is proportional to the number of gates (N_g) by the empirical relationship known as Rent's rule[7]: $(I/O) \sim (N_g)^{1/2}$.

In contrast, optical interconnections eliminate the RC delay while being free of reactive crosstalk and skew when compared with electronics. In addition, the optical approach does not require impedance matching resistors that increase the power requirements of the source electronics. Furthermore, optical interconnects increase circuit packing density by exploiting the third dimension in vertical I/O geometries, hence relaxing the pin-out limitation[8] viz. $(I/O) \sim N_g$.

Although optical interconnections have many advantages, the mature state of electronics technology cannot be ignored in constructing an interconnection system. Besides, due to inherently weak nature of optical non-linearities in solids, all-optical switching schemes face fundamental limitations. Therefore, the design of high performance, high bandwidth, processing-intensive switching networks requires that we take advantage of the strength of both optics and electronics[9]. These systems exploit the inherent parallelism and high bandwidth of optics while preserving the advantages of electronics in information processing, such as a high degree of integration, functionality, and gain. These optoelectronic schemes are envisioned as two dimensional islands of optically interconnected electronic processing arrays[10]. Each array consists of individual optoelectronic pixels which have optical inputs and outputs, with the processing being performed electronically.

Thus, the function of a single interconnect pixel is to first convert the optical input data into an electrical signal using a detector. The signal is then processed, reconverted to an optical signal, and then transmitted to the next stage. The function of the pixel is generalized by the block diagram shown in Fig. 1.1. The routing of optical signals can be done via bulk optics,

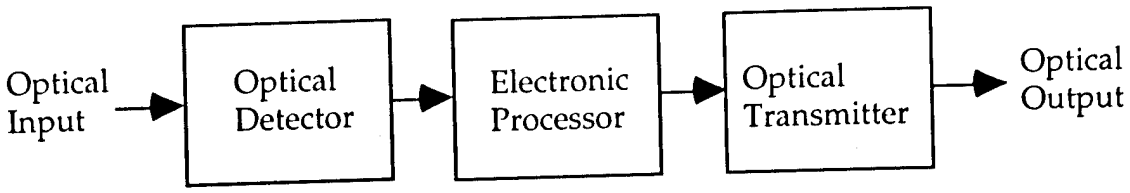

Fig. 1.1: The block diagram describing the general function of a smart pixel.

holograms, or fibers. These interconnection pixels, with some level of functionality are commonly referred to as "smart pixels".

The "intelligence" of the pixels, which are typically laid out in 2-D arrays, arises from their ability for performing logic or routing, depending on the nature of the incoming signal. There are currently four major lines of investigation of smart pixels[11]: (i) optoelectronic integrated circuits with detectors, transistors, and lasers or modulators in each pixel (ii) multiple-quantum-well self-electrooptic effect devices (or SEED's), (iii) vertical detector/emitter switches, and (iv) liquid crystal light valves integrated with Si VLSI. Our focus in this work is mainly on pixels of type (i).

The requirement of 2-D arrays for many smart pixel applications gives rise to important design issues: Power dissipation determines packing density (thus the I/O throughput), bandwidth determines the bit rate for the system, gain is required in any cascaded multi-stage network, and sensitivity determines the switching energy for the system. Furthermore, the arrays need to be produced in large quantities and with acceptable cost. The smart

pixel optoelectronic interconnections may be hybrid or integrated. In the fully hybrid approach, discrete components are optimized individually and then connected together using flip-chip or wire bonding. The wiring of discrete optoelectronic devices, however, includes laborious optical alignment processes that not only reduce the system reliability (yield), but also introduce reactances that may degrade bandwidth, as well as considerably increasing the system cost[12]. Thus, such hybrid systems are of limited use with the rapidly growing system requirements of optoelectronic interconnections.

These problems can be reduced by optoelectronic integration. Somekh and Yariv[13] in 1972 first mentioned the potential advantage of integrating an electronic processor, a laser and a photodetector on the same substrate. The first demonstration of an optoelectronic integrated circuit (OEIC) was in 1978, where Lee, et al.[14] integrated a laser with a Gunn-effect switch on a GaAs substrate. The integration of a photodiode and a transistor was first demonstrated on an InP substrate by Leheny, et al. [15] in 1980.

Compared to the hybrid approach, integrated interconnects are more compact while still maintaining high performance, function and manufacturability[16]. They do not rely on wire bonds, and hence can have low cost and reduced crosstalk, thus improving the bandwidth. These same advantages have driven the Si IC industry for the past quarter of a century. The materials used in fabricating OEIC's are selected from semiconductors such that both optoelectronic devices with useful operating wavelengths, and electronic devices can be readily fabricated on a common substrate. Furthermore, integration of optical devices on a common substrate provides

high efficiency optical coupling, thus in many instances avoiding complex optical alignment problems.

Thus, the design of a full functionality smart pixel needs to address issues related to integration, gain, bandwidth, packing density, and sensitivity.

It should be noted that material growth and processing challenges presented by integrating a variety of optical and electronic devices on a single chip greatly increase the fabrication complexity of modern OEIC's. While the performance of OEIC's is approaching that of the best hybrid circuits for certain low level computation and logic applications[17], schemes requiring high integration densities still rely on the hybrid approach due to the advanced state of Si processors[18]. In the long run, specific system requirements and applications will ultimately determine the choice of technology, and the regime for which it is suitable.

Potential applications of the OEIC technology in optical communication networks include *global* networks, *long-haul* networks, *wide area* networks, *local distribution* and *local area* networks, and *backplane* and *board level* interconnects. In this work, we mainly focus on smart pixels for use in back plane and board level interconnects which increase speed, reduce crosstalk and skew, and reduce the size, power, and weight of the interconnect compared to the electronic approach[11].

Cloonan, et al[19]. have proposed using 2-D smart pixel arrays for implementing a self-routing crossbar interconnect. The data stream in such systems includes a header which contains the routing information for that packet. The routing information determines the state (permutation) of each optoelectronic switching element. Once the electronic switch is completely

set, the optical packet (including the header and the data packet) is sent through the switch. These networks are capable of performing a perfect shuffle, which is required by many computer hardware arrangements (such as fast-Fourier-transform processors and cross-point switches). In such a cascaded network, any input may be directed to any output, and all inputs are directed to distinct outputs. The diagram for such a system is shown in Fig. 1.2. Crossbar networks require a large number of logic gates for switching elements, and also require a large number of links to interconnect these elements. These two facts have been viewed as major limitations for the electronic implementation of large crossbar networks. However, the high pinout capabilities of optical chip-to-chip interconnection hardware afforded by smart pixels which can read addresses and route packets in real time helps to alleviate the interconnect limitation.

Another potential application for smart pixel arrays was proposed by Prucnal[20] in high-functionality, self-routing 2-D lattice networks, which have synchronization and contention resolution. In such systems, resolving the contention of packets at multiple input ports for a single output port is done according to an established priority scheme, in a manner that minimizes packet loss. Packets are also synchronized at the input.

Sawchuk, et al[21]. proposed using 2-D arrays of smart pixels as spatial light modulators (SLM's), where they can modulate intensity, wavelength, or polarization of the light. Such systems combine the amplification, functionality and array geometry of traditional SLM's, with many additional capabilities provided by the on-chip electronic processing of the smart pixels.

An 8x8 optoelectronic crossbar switch, was demonstrated by Forrest, et al.[22] in 1989. We propose to use smart pixels using electrical or optical

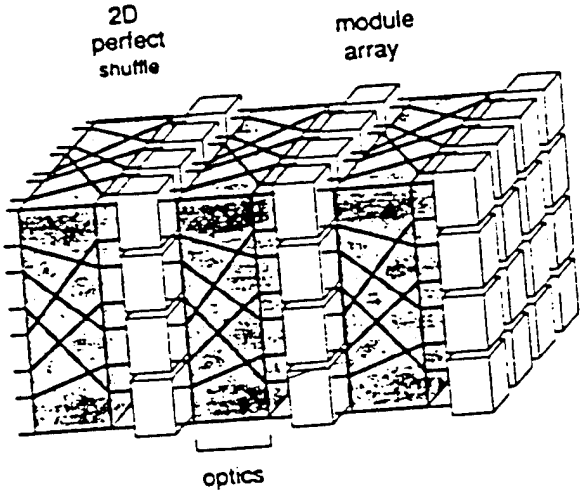

Fig. 1.2: The diagram for a two-dimensional perfect shuffle multistage interconnection network (Ref. [23]).

control to replace the nodes in such a system. The added functionality of the pixel (such as high sensitivity, thresholding function, and gain which is needed for fanout) will enhance the overall processing capabilities of the networks described.

The size of an interconnect system is largely limited by the loss and by the detector sensitivity at each stage. For a multi-stage network, the loss at each stage is the result of inefficient optics (microlens arrays or holograms), the optical-to-electrical conversion loss of the pixel input, losses in the circuit due to various noise contributions, and the electrical-to-optical conversion loss at the output. The number of stages allowed will, therefore, be limited by the sensitivity of each pixel, i.e. the minimum power it can detect while maintaining a fixed signal-to-noise ratio (in an analog case), or bit error rate (abbreviated BER, for a digital case). One way to alleviate this restriction is for each pixel to have gain. If the gain is large enough, the number of cascaded stages in an interconnect may no longer be limited by pixel sensitivity. Furthermore, gain and sensitivity determine the fanout for each pixel in systems where fanout is required.

A central criterion in evaluation and comparison of different interconnect schemes is the energy required for switching. Switching energy is a combined measure of the sensitivity and switching time (bandwidth) of the system. At low temperatures, switching energy and sensitivity can be improved due to the reduction in circuit noise, and improvement in conversion efficiencies in the pixel. Likewise, at higher circuit temperatures (which may result from large power dissipation), the system performance can noticeably degrade[24].

In this thesis, we demonstrate a hybrid/integrated optoelectronic smart pixel. The functionality of this circuit includes amplification and switching (both linear and thresholding) with an electrical control. Generic smart pixels include some logic functions, such as routing. Although the smart pixel demonstrated here constitutes limited functionality, it addresses many of the same issues for a full-function pixel. These include integration, gain, packing density, bandwidth and sensitivity. The smart pixel was designed to optimize the performance with regard to all of these issues.

Our circuit includes a laser output source, gain, and cascadability. The circuit was fabricated in the InP/InGaAsP material system (λ=1.3 μm, grown using gas source molecular beam epitaxy, GSMBE), hence making it compatible for use at the interface of long wavelength fiber-optic networks and board-level optoelectronic interconnections. Another goal was to advance the fabrication technology in the relatively novel InP-based materials system. Furthermore, many of the electronic devices in this material system are superior to their GaAs counterparts[25].

The contribution of this thesis is in exploring the issues related to optoelectronic smart pixels, in particular, the switching energy. The pixel demonstrated here has the lowest switching energy obtained to date for comparable technologies[26-29]. This was achieved while trying to optimize the other pixel figures of merit, i.e. gain, low power dissipation, and bandwidth. We have also performed a theoretical noise analysis to predict the sensitivity (thus switching energy) limits in several detection schemes as a function of bit rate and temperature, and found schemes with optimum sensitivity.

A further contribution of our work includes advances in fabrication technology, furthering the limits of material processing in long wavelength OEIC's. This was accomplished by demonstrating the feasibility of a hybrid/integrated configuration for the smart pixel receiver/transmitter, in which the photodetector and the electronic components were integrated, and the output laser was surface bonded onto the transistor circuit chip. This circuit, therefore, lays the groundwork for future all-integrated (monolithic) transceiver circuits. Some of the work presented here has been published elsewhere[30-32].

This dissertation is organized as follows: In Chapter 2, we discuss the pixel circuit design based on analytical techniques and computer simulations. In Chapter 3 material growth and fabrication steps for the pixel are discussed. Chapter 4 includes the experimental results on the performance of the pixel. Also included in this chapter are low-temperature results on the performance of discrete pixel components. In Chapter 5 we calculate and compare the performance of different receiver types for different regimes of temperature and bit rate. In Chapter 6, we present conclusions and discuss the future work. Appendix A includes details of the circuit analysis. The SPICE simulation parameters and program files are presented in Appendix B. Appendix C contains complete details of the pixel fabrication in process sheets, and Appendix D includes the photolithographical mask layout.

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Chapter 2

Design of the smart pixel circuit

2.1 Introduction

As discussed in Ch. 1, optoelectronic (OE) smart pixels are crucial building blocks for implementing large scale, free space or fiber optical interconnects. In such systems, optics is used to transmit data, while electronic processors within each pixel perform various logic functions[1,2]. The range of functionality for smart pixels includes optical switching, amplification, logic, modulation, and signal routing[3].

In this chapter, we discuss the design of an optical interconnect unit, to be referred to hereafter as the smart pixel. In section 2.2, the requirements and performance targets for the design of optoelectronic smart pixel switches are discussed. We then propose a design and perform detailed circuit analysis in order to evaluate the functionality of the unit in section 2.3. In section 2.4 the required performance by discrete pixel components is discussed.

2.2 Design requirements for smart pixels

2.2.1 Performance requirements

There are many critical issues in the design of OE smart pixels which need to be addressed individually and optimized for different applications. Table 2.1 contains a list of crucial design parameters and the performance

Table 2.1

List of smart pixel performance requirements

Parameter	Significance	Desired Setting
geometry	I/O	vertical
cascadability (R)	limits the number of cascaded stages	>1
operation wavelength (λ)	compatibility with long distance fiber networks	1.3 μm
dissipated power density	limits packing density	< $1W/cm^2$
switching energy	characterizes bandwidth, sensitivity, and fan out	~ 1 fJ
temperature sensitivity	affects laser I_{TH}	higher T_0
speed	operational bandwidth	~ 100 MHz
optical large signal gain	limits fan-out	> 2
optical small signal gain	amplification	~ 10
contrast ratio	limits bandwidth	high

targets based on the system requirements. Here, we further explain the importance of each point.

The input/output (I/O) geometry in an optical interconnection is significant for the system functionality. Pixels containing edge emitting transmitters suffer from I/O restrictions stemming from their fabrication geometries. High-efficiency low threshold current edge-emitting lasers are fabricated by cleaving both the front and the rear laser facets. If this form of facet formation is employed, all peripherally integrated circuits would have to be confined to a chip of the same length as the laser (generally 200-300 μm long)[4]. These restrictions limit the pixel packing density, and hence, the scale of integration. It is fair to say that with edge emitting transmitters, one major advantage of optics, i.e. the use of the third dimension, is lost. The desire to fully exploit the advantages of optics has motivated extensive research in the area of vertical surface emitting optical transmitters. These devices include the folded cavity surface emitting lasers (FCSEL's)[5], and the vertical cavity surface emitting lasers (VCSEL's)[6]. For long wavelength applications, FCSEL's demonstrate better threshold current and slope efficiency than their VCSEL counterparts[5].

Another important factor is cascadability. We refer to the parameter used to characterize this factor as R. This parameter is defined as the ratio of the output on-off power levels to that of the input. The expression for R, and the condition of cascadability are defined below:

$$R = \frac{Output\ on/off}{Input\ on/off} \geq 1 \qquad (2.1).$$

In order to further understand cascadability, let us look at the Figure 2.1 (a), (b). In Fig. 2.1(a), the output on/off ratio is larger than that of the input, or R>1. Hence, the output of this stage can drive the following stages in a cascaded multilayer system. However, in the case shown in Fig. 2.1 (b), R<1. This implies that if this output is to drive the next stage, the output of the second stage will have an even worse on/off ratio. Therefore, the on-state power will gradually diminish towards the off state, and the two will eventually become indistinguishable. Subsequently, the signal will be lost after a few stages.

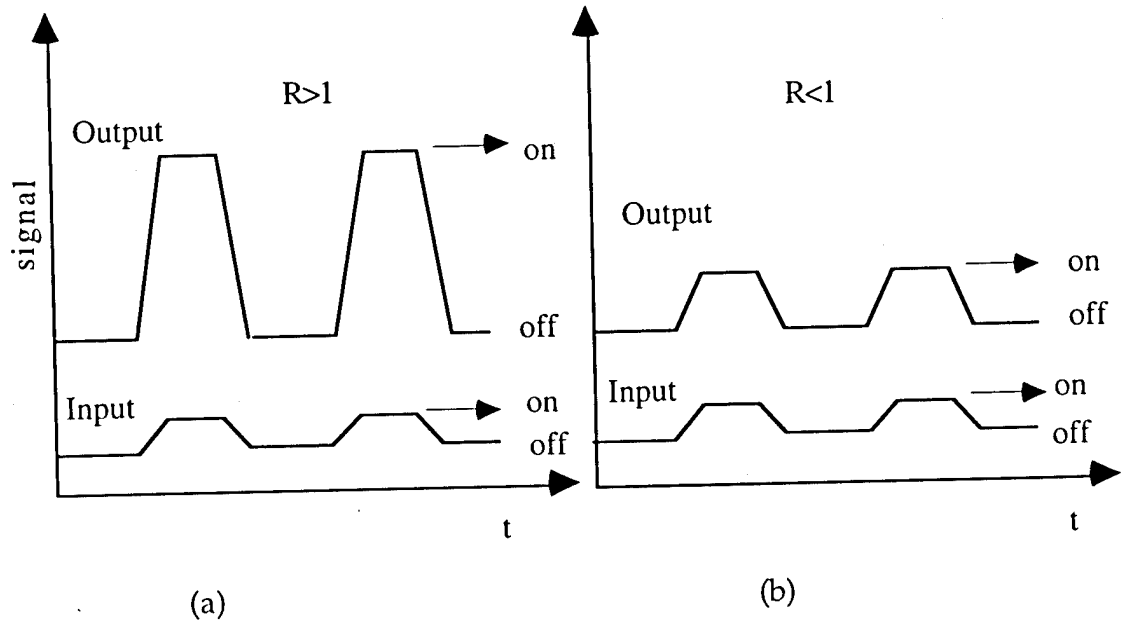

Fig. 2.1: Demonstration of the condition for cascadability.

Another criterion in the design of optical interconnects is the operation wavelength. As mentioned in Ch. 1, the signal wavelength will determine the distance range for which the interconnect is most suited. In

long distance fiber optics communication, 1.3 μm or 1.55 μm are the wavelengths of choice. The reason is that silica fibers have the lowest dispersion and loss at these wavelengths.

Even at the optimum wavelengths, there is non-negligible propagation loss. Amplifiers need to be placed along the transmission path to compensate for this loss. The distance between these stations is determined by the receiver sensitivity[7], P_{min}. This parameter is a measure of the minimum time averaged power required to achieve switching for a desired signal to noise ratio (for an analog case) or bit error rate (abbreviated to BER, for a digital case). Higher receiver sensitivities allow fewer amplifiers, and hence, result in reducing the system cost.

The sensitivity of a pixel is also important in its role in determining the circuit fan-out. That is[2]:

$$P_{min} \leq \frac{P_{out}\eta_c}{F} \tag{2.3}$$

where P_{out} is the output power, η_c is the optical coupling efficiency, and F is fanout. It is seen from Eq. 2.2 that for a fixed output power, fanout will increase for improved sensitivity, i.e. lower P_{min}.

A parameter often used to compare different interconnect technologies is the switching energy, E_{sw}. This parameter is a combined measure of the bandwidth (Δf) and the sensitivity of the device and is defined as follows:

$$E_{sw} = P_{min}/\Delta f \tag{2.4}.$$

By definition, it is clear that lower E_{sw} devices are desirable as they demonstrate better sensitivity or higher bandwidth, or both. Switching energies as low as 1 fJ have been demonstrated for hybrid[8] as well as

monolithically integrated[9] photoreceivers. Smart pixels which include transmitters, have this added functionality compared to stand-alone photoreceivers. This implies that in order to optimize smart pixel performance, not just sensitivity, but additional factors such as optical gain need to be taken into account. Therefore, the switching energy of smart pixels will in general be higher than that of receivers. In setting the design goals for the smart pixels, the target switching energy is ~ 1 fJ.

In practice, devices are never thermally isolated. A device is affected by the heat generated from nearby devices, and that generated from the device itself. It will be shown in Ch. 4 that the performance of transistors and photodetectors varies with temperature. In optoelectronic interconnects, temperature sensitivity is especially important for quantum well devices such as lasers or the SEED device[10]. The temperature dependence of the threshold current of the output laser is[11]:

$$I_{TH}(T) = I_{TH0}\, exp\ (T/T_0) \tag{2.5}$$

where I_{TH0} is the temperature independent part of the threshold current, and T_0 is the characteristic temperature. Higher T_0 implies a smaller variation of I_{TH}, and hence smaller temperature sensitivity for the pixel. Furthermore, temperature sensitivity of a device can dictate the permitted power dissipation, hence the number of devices per unit area, referred to as the "packing density", ρ.

Among the major advantages of optics are high bandwidth and parallelism of channels (Ch. 1). Although various application exploit different device characteristics, the system performance is most accurately assessed by including both of these factors. The maximum amount of

information flowing through a system is the information flux (Φ) defined as[2]:

$$\Phi = \Delta f \rho \qquad (2.6).$$

Eq. 2.6 demonstrates the importance of bandwidth and packing density in determining the total system capacity. The maximum tolerable dissipated power in semiconductors with passive cooling is 1 W/cm^2. If we assume the same I/O density for smart pixels as for Si VLSI, i.e. 100/cm^2, the allowed power dissipation per pixel is 10 mW. It should be pointed out that in many applications, the percentage of the total area occupied by the optical I/O will decline as the amount of functionality per pixel is increased. If the number of optical I/O's remain large, the packing density will be further limited by the cost and complexity of the optical imaging system used[12].

One major criterion in the design of an optoelectronic switch is the optical input/output (I/O) gain. The large signal (DC) gain is defined as:

$$G = \frac{P_{out}(on)}{P_{in}(on)} \qquad (2.7).$$

Gain is required for each interconnect stage to compensate for coupling and transmission losses, and hence will determine the number of fanout stages (F) that can be driven by the output signal. The condition to achieve fanout for a coupling efficiency of η_c is[3]:

$$G \geq \frac{F}{\eta_c} \qquad (2.8).$$

It can be seen that higher gain allows for larger fanout. Small signal gain of the circuit is defined as:

$$g = \frac{d(P_{out}(on))}{d(P_{in}(on))} \qquad (2.9).$$

This gain is a measure of the signal amplification that the switch can provide. Generally, for OEIC's, g ~10 is considered sufficient[2] .

An important parameter to characterize pixel performance is the contrast ratio, defined as the ratio of output power in the on and off states :

$$CR = \frac{P_{out(on)}}{P_{out(off)}} \qquad (2.10).$$

In practice, $P_{out(off)}$ is not much smaller than $P_{out(on)}$ due to parasitic effects and the limited circuit gain. High contrast ratios are crucial to interconnect systems, as they assure less inter symbol interference. This results in improved bandwidth, and further amplifier spacing in case of long distance links.

2.2.2 Choice of materials and devices

To fabricate a monolithically integrated pixel for use at 1.3 μm and 1.55 μm wavelengths, the optical as well as the electronic circuit components need to be based on InP-related compounds. The use of these materials, however, introduces a limitation in the types of electrical devices that can be employed. The low Schottky barrier heights formed on InP and InGaAs prohibit the fabrication of high performance metal-semiconductor field-effect transistor (MESFET)[13]. In addition, the high surface state density of InP/insulator interfaces induces drain-current drift often leading to unstable metal-insulator-semiconductor field-effect transistor (MISFET)[14] characteristics. Due to these limitations, junction field-effect transistor (JFET)[15] or

heterojunction bipolar transistor (HBT)[16] technologies have been widely pursued in InP-based materials[17].

The higher transconductance of bipolar transistors as compared to field effect transistors (FET's) at the same quiescent operating current results in bipolar amplifiers with smaller power dissipation[18]. The advantages of using HBT's versus homojunction bipolar transistors in high frequency optoelectronic circuits stem from (i) the freedom to increase the base doping (which results in lowering the base resistance and thus improving the bandwidth) without decreasing the emitter injection efficiency, (ii) the ability to reduce the emitter doping concentration (thus lowering the base-emitter depletion capacitance) without lowering β, (iii) and the lower base transit times due to the barrier in the conduction band for abrupt structures which may result in ballistic transport.

P-i-n photodetectors are capable of high bandwidth, high efficiency operation[3,19], and the p-i-n material growth and fabrication steps are compatible with HBT structures. An alternative to the use of p-i-n's in conjunction with HBT's at the receiver front end is using heterojunction phototransistors (HPT's)[20]. In order to optimize the optical coupling efficiency, the HPT area needs to be relatively large, which contributes to a large capacitance and hence lower bandwidth. Furthermore, the advantage of separating the p-i-n's and the HBT's is that each device can be individually optimized.

2.3 The Smart Pixel Circuit

2.3.1 Circuit Configuration and Operation

The smart pixel demonstrated in this work consists of a monolithically integrated receiver and a surface mounted optical output laser. The pixel was entirely implemented in InP/InGaAsP material system, and includes a total of nine optical and electrical devices: a p-i-n photodetector, three HBT's, two semiconductor resistors, two metal thin film resistors, and a folded cavity surface emitting laser (FCSEL). The p-i-n photodetector at the input stage is followed by an HBT-based transimpedance amplifier at the front end. The output stage is an HBT differential pair which produces transconductance gain as well as provides the output signal current as a function of the input optical power. It also forms the decision making part of the circuit. The output device is a FCSEL. The circuit diagram of the pixel is shown in Fig. 2.2.

An optical input signal at the p-i-n produces a current that results in a negative voltage swing at the base of Q_2. This voltage swing gives rise to a current swing in the collector of Q_3 in the differential pair. This increase in the output laser current will then increase the emitted optical power.

The front end consists of a transimpedance amplifier with feedback resistor, R_f. Negative feedback stabilizes the amplifier gain against parameter changes such as current gain, supply voltage variation, or temperature changes[21]. Furthermore, negative feedback produces an increase in the bandwidth of the amplifier.

The differential pair also helps to ensure stable performance that is relatively insensitive to individual device characteristics, resulting in high processing yields. The output stage contains the FCSEL and its external bias

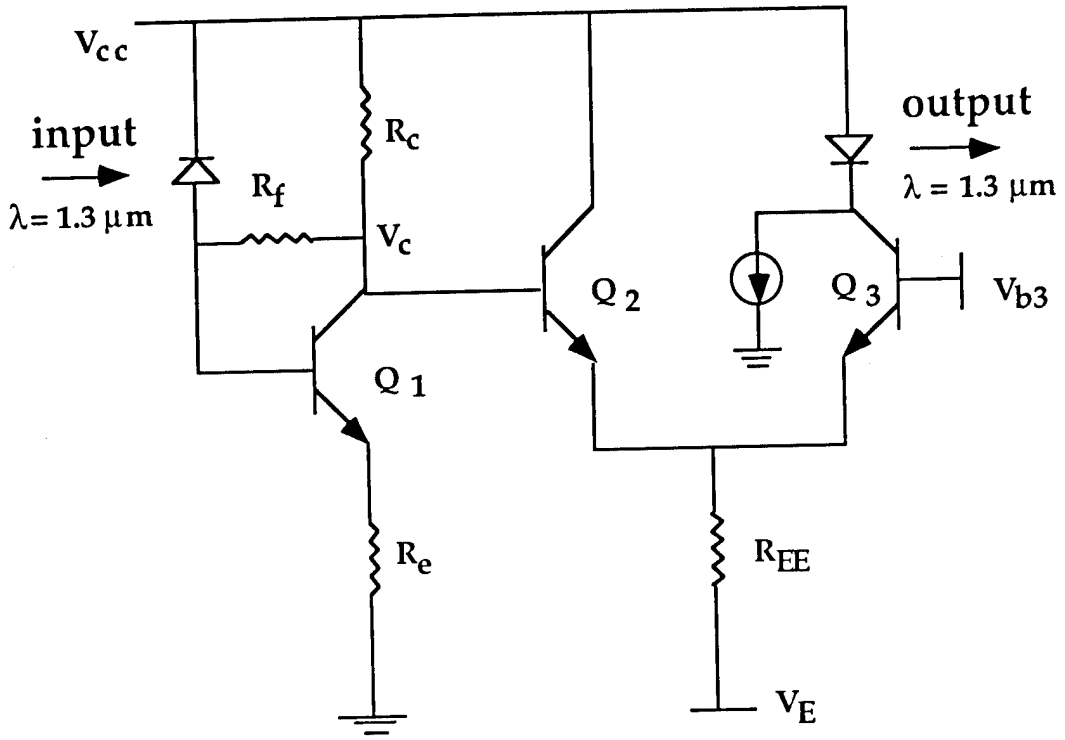

Fig. 2.2: The circuit diagram of the smart pixel.

circuit. By keeping the laser just at or above threshold, the switching action increases the emitted output power instead of turning the laser on from a below-threshold off state. This method of pre-biasing provides a control mechanism to enable and disable the switch. Furthermore, it results in higher bandwidth, since the capacitors associated with the laser do not need to fully charge and discharge at each cycle. The drawback, however, is that the pre-bias gives rise to a quiescent power dissipation, which is usually a large fraction of the total power dissipated in the circuit.

2.3.2 Circuit Analysis

The values of components used for the smart pixel circuit were selected in order to optimize three major criteria which are considered as the figures of merit of the pixel: These are bandwidth, power dissipation, and gain. Table 2.2 contains the list of component values used for our smart pixel modeling. The effect of each component on these figures will be discussed later.

The light signal detected by the p-i-n gives rise to a photo current, I_{ph}. Most of I_{ph} flows through the feedback resistor, R_f, with only a small fraction of I_{ph} flowing through the base of Q_1. The ratio of the signal induced currents through the feedback resistor and the base (I_{fs}, and I_{bs}, respectively), as shown is Appendix A is:

$$\frac{I_{fs}}{I_{bs}} = \frac{\beta R_c}{R_f + R_c} \qquad (2.11).$$

The current I_{fs} flowing though the feedback resistor gives rise to a negative voltage swing at the output of the front end, pulling the base of Q_2 down. It

Table 2.2

Component values for the smart pixel circuit

Component	Definition	Value
V_{cc}	supply voltage	3.0 V
V_{EE}	diff. pair emitter voltage	-1 V
V_{b3}	bias applied to base of Q_3	0.85 V
R_f	feedback resistor	7 KΩ
R_c	collector resistor	2 kΩ
R_e	emitter resistor of front end	200 Ω
R_{EE}	diff. pair emitter resistor	150 Ω

is shown in Appendix A that the photocurrent and the change in the front end voltage swing are related via:

$$I_{Ph} = -\Delta V_c\left(\frac{R_c(1+\beta)+R_f}{\beta R_c R_f}\right) \tag{2.12}$$

where R_c is the collector resistor and β is the transistor common emitter current gain. For β>100 Eq. 2.12 can be simplified as:

$$\Delta V_c = -I_{Ph}R_f \tag{2.13}$$

$$\text{where } I_{ph} = \frac{q\lambda\eta_c\eta_{ph}}{hc}P_{in} \tag{2.14}.$$

In the above equation, η_c is the optical coupling efficiency, and η_{ph} is the detector external quantum efficiency. Although β affects the front end voltage swing, its role is small for high β values (Eq. 2.12). However, for small β, ΔV_c starts to deviate from the value predicted by Eq. 2.12. For example, when β drops to 20, the values of ΔV_c will be higher than that predicted in Eq. 2.12 by about 5%. The dependence of $\Delta V_c/I_{ph}$ ratio on β is found from Eq. 2.12 to be:

$$\frac{\partial\left(\frac{\Delta V_c}{I_{ph}}\right)}{\partial\beta} = \frac{-1}{\beta^2(R_c \| R_f)} \tag{2.15}.$$

This further demonstrates the need for higher values of β.

The analysis here includes results obtained using a circuit simulation package, Intusoft SPICE, version 4. SPICE requires many device parameters to perform the calculation, which were obtained experimentally from our

own discrete device data, or calculated. Appendix B contains a list of parameters used for these simulations and the circuit files.

Fig. 2.3 shows the SPICE simulation results for the front end output (V_c) voltage swing. According to this graph, for an input optical power swing of 50 μW, the output of the front end changes by about 0.25 V. For values of input power >50 μW, Q_1 saturates, and V_c levels off. The front end voltage change is effectively a swing in the base of Q_2 of the differential pair. The base of Q_3 is fixed externally at a voltage in the middle of the swing range of V_{b2}, i.e. at 0.85 V. The relative magnitudes of the collector currents of Q_2 and Q_3 (referred to as I_{c2} and I_{c3}) depend on the difference in base voltages of these two transistors, Q_2 and Q_3. Before any input is detected, $V_{b3}<V_{b2}$, and hence, $I_{c3}<I_{c2}$. This implies that the laser is in the 'off' state. Once the input is detected, the base of Q_2 swings below V_{b3}, resulting in a positive swing in the collector current of Q_3, i.e. $I_{c3}>I_{c2}$. Fig. 2.4 demonstrates the change in I_{c2} and I_{c3} as a function of optical input power. The change in I_{c3} is:

$$\Delta I_{c3}=g_{md}\Delta V_c/2 \qquad (2.16).$$

where g_{md} is the differential pair transconductance, and from Fig. 2.4, its value is to be found to be 5 mS.

In most differential pairs, a current source is placed at the emitter, keeping the sum of $I_{c2}+I_{c3}$ a constant. This current source is usually another bipolar transistor. In our design, however, to maintain simplicity we have placed a resistor at the emitter. Therefore, the sum of the two currents will no longer be constant, as the emitter voltage, and hence the current in R_{EE}, changes with input power. That is the reason for the observed asymmetry

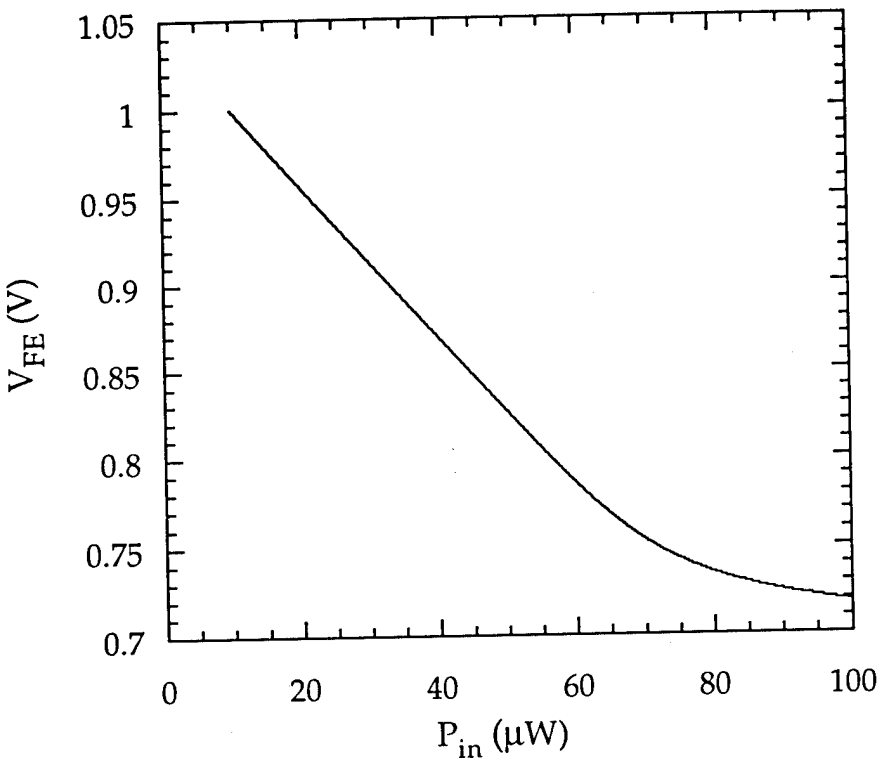

Fig. 2.3: The simulated output swing of the front end.

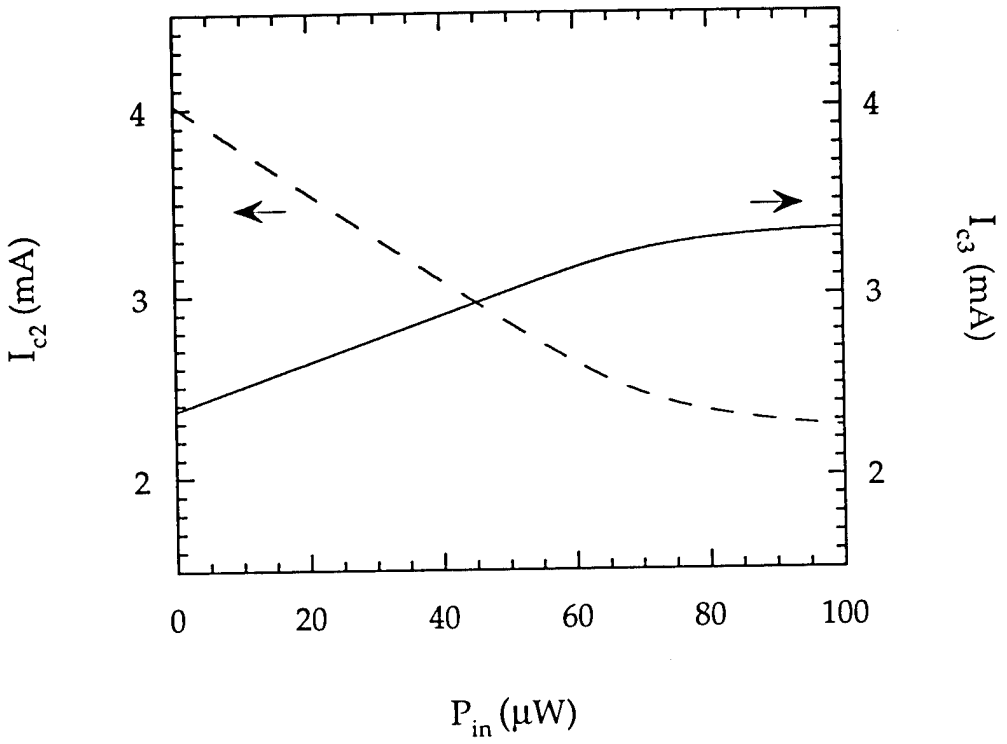

Fig. 2.4: The simulated plot of currents of the differential pair.

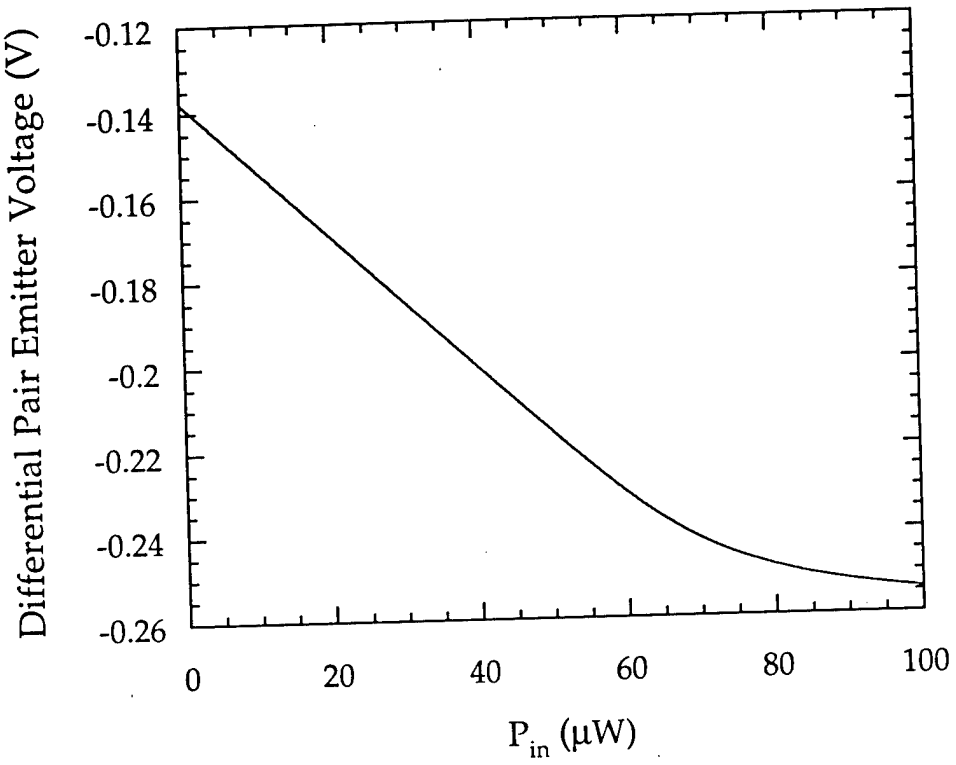

Fig. 2.5: The simulated change in the emitter voltage of the differential pair transistors

between I_{c2} and I_{c3} in Fig. 2.4. Fig. 2.5 shows the change in the differential pair emitter voltage as a result of the optical input power. It is expected that in this case, $\Delta I_{c3} = \Delta I_{c2} - \Delta I_{REE}$, or: $\Delta I_{c3} = \Delta I_{c2} - \Delta V_{EE}/R_{EE}$. The results shown in Figs. 2.4 and 2.5 confirm this expectation.

Fig. 2.6 shows the change in the output optical power as a result of the input power swing. From the plot, we deduce G~3. The expected output power can be calculated using the following expression:

$$P_{out(on)} = \frac{hc}{q\lambda}\eta_d(I_{on} - I_{prebias}) + P_{out(off)} \qquad (2.17)$$

where η_d is the laser slope efficiency, h is Planck's constant, c is the speed of light in vacuum, q is the electron charge, and λ is the wavelength, I_{on} is the current through the laser in the on state, and $I_{prebias}$ is the current applied to the laser to keep it near threshold, and:

$$P_{out(off)} = \frac{hc}{q\lambda}\eta_d(I_{prebias} - I_{TH}) + \eta_{sp}I_{TH} \qquad (2.18)$$

where η_{sp} is the spontaneous emission efficiency, and I_{TH} is the laser threshold current. Let us now consider a hypothetical case, where the laser threshold current and the pre-bias current and the collector current of Q_3 in the off state are all equal, namely: $I_{TH}=I_{prebias}=I_{c3\,(off)}$. Then,

$$P_{out(on)} = \frac{hc}{q\lambda}\eta_d(I_{on} - I_{TH}) + \eta_{sp}I_{TH} \qquad (2.19).$$

In the above expression, $I_{on}-I_{TH}=\Delta I_{c3}$. Since $\eta_{sp} << \eta_d$, the second term in Eq. 2.19 can be ignored, and therefore,

$$P_{out(on)} = \frac{hc}{q\lambda}\eta_d\Delta I_{c3} \qquad (2.20).$$

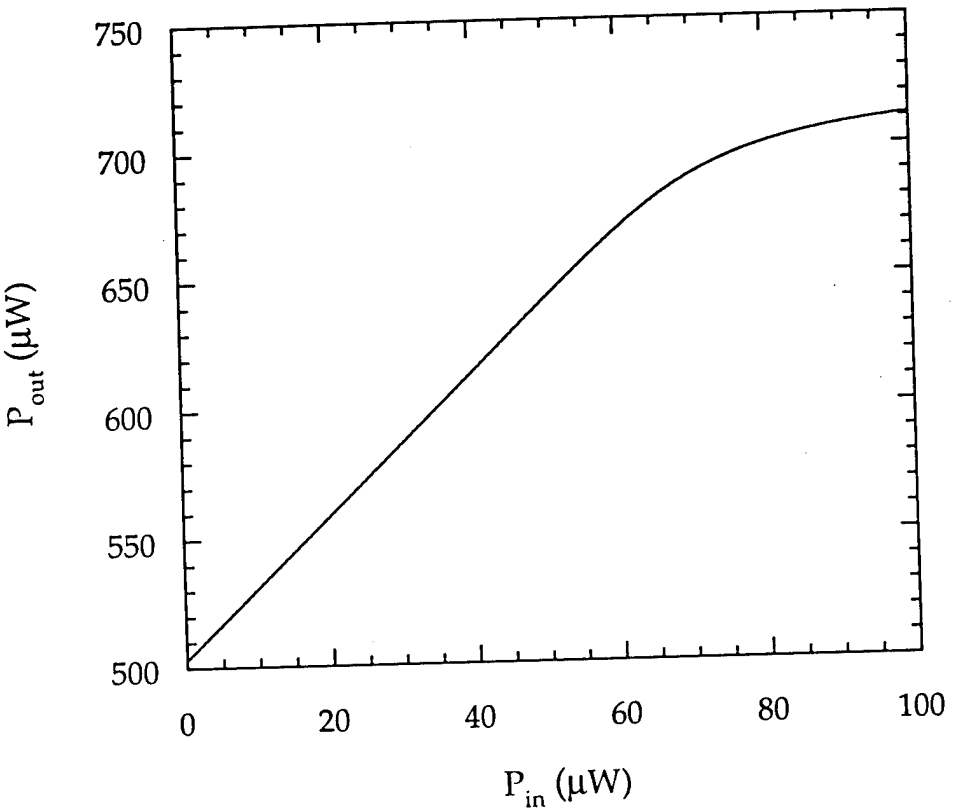

Fig. 2.6: The simulated output swing of the pixel.

Substituting for ΔI_{c3} using Eq. 2.12, 2.13, and 2.14 we can calculate the value of large signal gain as:

$$G = \frac{P_{out(on)}}{P_{in(on)}} = \frac{1}{2}\eta_c \eta_d \eta_{ph} g_{md} R_f \approx 2.5 \qquad (2.21).$$

where η_c is the coupling efficiency, η_{ph} is the detector external quantum efficiency, and g_m is the transconductance of the differential pair. The value of G calculated here is slightly lower than the value of 3 obtained from SPICE, due to the approximations that we made in the hand analysis. The contrast ratio can be expressed as $P_{out(on)}/P_{out(off)}$ is almost infinite, as $\eta_{sp} << \eta_d$.

In the above calculations, we have assumed η_d=17% and $\eta_c\eta_{ph}$=80%. Eq. 2.21 shows that the smart pixel is linear with the input signal for the power range prior to its saturation. The pixel can also be operated as a thresholding circuit by applying large enough input power levels to push it into saturation. However, the bandwidth degradation in this case, may limit the pixel functionality.

In order to calculate the frequency roll off for the pixel, we used the hybrid-π equivalent circuit shown in Fig. 2.7. In this model, r_{bb} is the base resistance, which in this model includes the base sheet resistance and the contact resistance. The base-emitter capacitance, C_π, consists of the depletion and the diffusion capacitances of the forward biased junction, C_P is the p-i-n capacitance, r_P is the p-i-n series resistance, C_μ is the base-collector junction capacitance, and $g_m = qI_c/kT$ is the HBT transconductance. The internal series resistances of the emitter and the collector, r_e and r_c, are usually small and have been ignored in this analysis. In the small signal model presented here, the resistance and capacitance of the differential pair have been lumped into

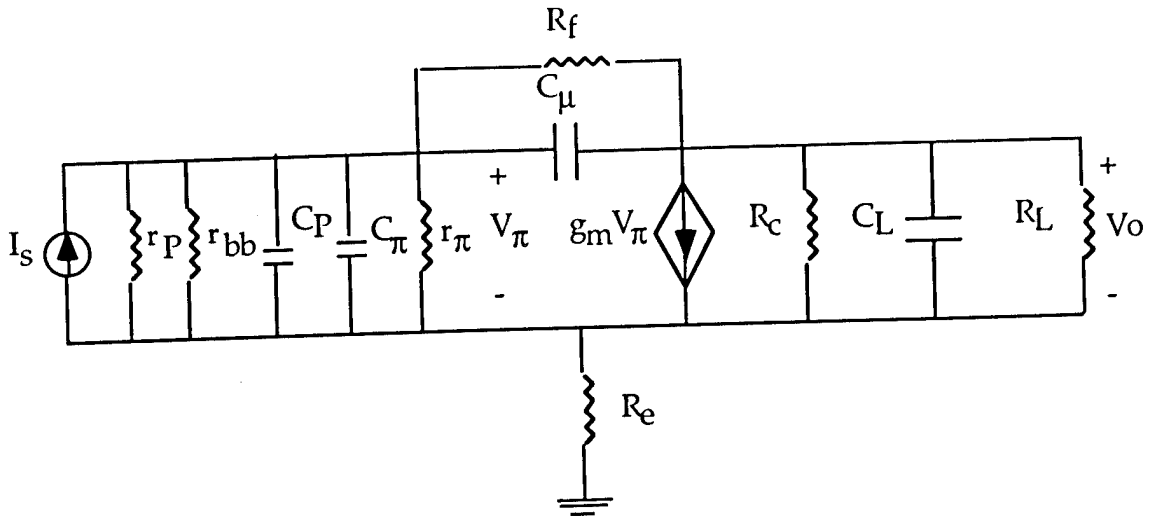

Fig. 2.7: Small signal equivalent circuit for the smart pixel. The impedance of the output stage is lumped in R_L and C_L.

R_L and C_L, respectively. The resistance, R_L is the combination of base-emitter-junction and emitter internal resistances of the differential pair transistors, Q_2 and Q_3. Likewise, C_L is the series combination of base-emitter junction capacitances of Q_2 and Q_3 in parallel with the base-collector junction capacitance of Q_2.

The small signal circuit presented in Fig. 2.7 can be simplified to the model in Fig. 2.8. Here, R_f is broken into R_{f1} and R_{f2} using Miller's theorem. Likewise, $C\mu$ is broken into $C\mu_1$ and $C\mu_2$. The voltage gain of the circuit, K, is:

$$K = \frac{V_o}{V_\pi} = \frac{Z_L(1 - g_m Z_f)}{Z_L + Z_f} \approx -g_m Z_L \| Z_f \tag{2.22}$$

where $Z_L = R_{cL} \| C_L = \dfrac{R_{cL}(1/sC_L)}{R_{cL} + 1/sC_L}$ and $Z_f = R_f \| C_\mu = \dfrac{R_f(1/sC_\mu)}{R_f + 1/sC_\mu}$.

Hence, using Miller's theorem we can write:

$$R_{f1} = \frac{R_f}{1-K} \qquad (2.23)$$

$$R_{f2} = \frac{R_f}{1-1/K}$$

Similarly,

$$C_{\mu 1} = C_\mu(1-K) \qquad (2.24).$$

$$C_{\mu 2} = C_\mu(1-1/K)$$

Furthermore, we have combined the other circuit components as follows:

$$r_{\pi bP} = r_\pi \parallel r_{bb} \parallel r_P,\ C_{\mu 1\pi} = C_{\mu 1} \| C_\pi \| C_P, \qquad (2.25)$$

$$C_{\mu 2L} = C_{\mu 2} \| C_L,\ R_{cL} = R_c \| R_L$$

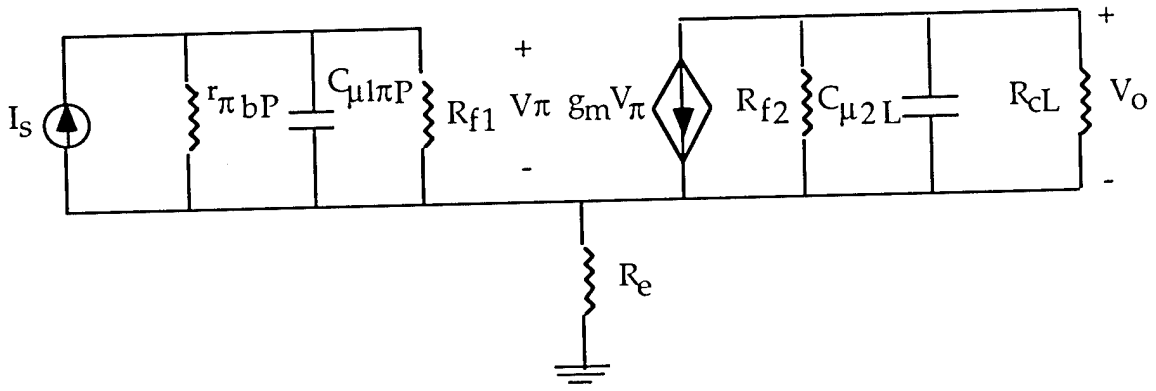

Fig. 2.8: The simplified small signal equivalent circuit for the smart pixel.

The values used for the small signal model parameters are presented in Table 2.3. We can then obtain the frequency response of the circuit by calculating the poles ω_1 and ω_2 (one from each half of the circuit) of the circuit transfer function. These poles can be written as:

$\omega_1 = [C_{\mu 1\pi P}(r_{\pi bP} \| R_{f1})]^{-1}$

$\omega_2 = [C_{\mu 2L}(R_{cL} \| R_{f2})]^{-1}$.

Fig. 2.9 shows simulated frequency roll off, resulting in bandwidth of 81 MHz.

Table 2.3

List of circuit parameters used for the small signal model of the pixel

Parameter	Definition	Value
r_{bb}	base sheet and contact resistance	1 kΩ
r_{π}	base-emitter resistance	5.2 kΩ
$r_{\pi bP}$	$r_{\pi}\|\|r_{bb}\|\|r_P$	160 Ω
C_{π}	base-emitter capacitance	400 fF
C_{μ}	base-collector capacitance	300 fF
R_{f1}	effective R_f at input	---
R_{f2}	effective R_f at output	---
g_m	transconductance	40 mS
C_L	load capacitance	500 fF
R_L	load resistance	4 kΩ
R_{cL}	$R_c\|\|R_L$	1.3 kΩ
r_P	p-i-n series resistance	200 Ω
C_P	p-i-n capacitance	100 fF
$C_{\mu 1}$	effective C_{μ} at input	---
$C_{\mu 2}$	effective C_{μ} at output	---
$C_{\mu 1\pi P}$	$C_{\mu 1}\|\|C_{\pi}\|\|C_P$	---
$C_{\mu 2L}$	$C_{\mu 2}\|\|C_L$	---

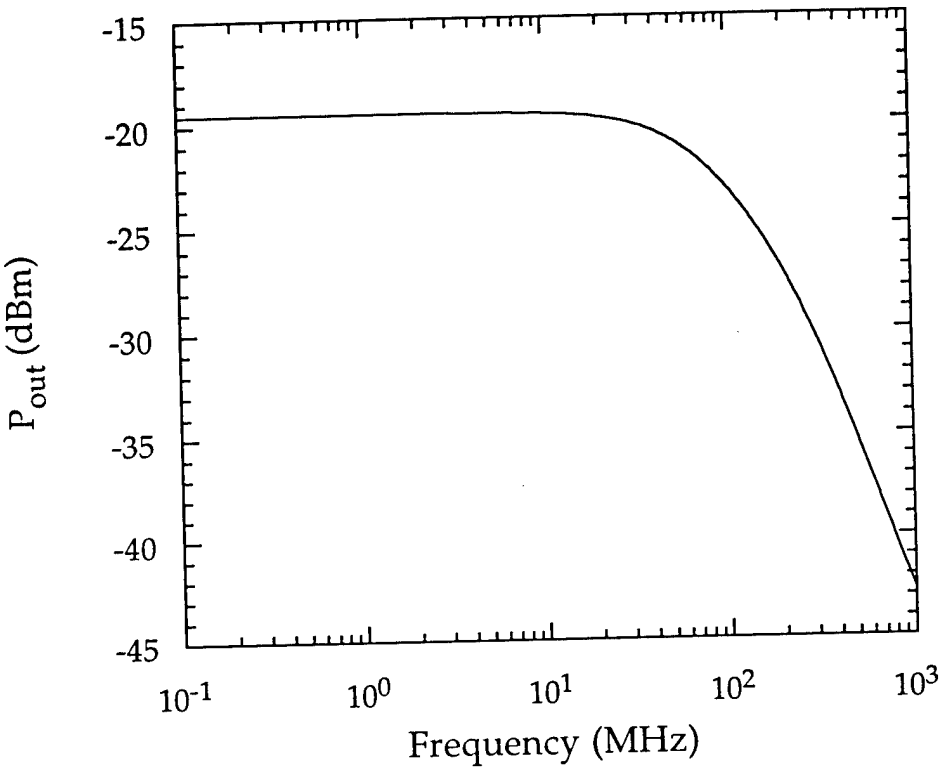

Fig. 2.9: Simulated frequency response of the circuit from SPICE analysis.

2.3.3 Effect of component values

We now look into the effects of individual circuit parameters in determining the three figures of merit of the smart pixel. It was mentioned earlier in this chapter that the component values are chosen to optimize optical gain, bandwidth and power dissipation. In this section, we study the effect of changing one component value at a time, while keeping all the other parameters the same as in Table 2.2. We first consider the effect of the feedback resistance. The pixel frequency response for different values of R_f is plotted in Fig. 2.10. The results are summarized below:

R_f (kΩ)	Gain	Bandwidth (MHz)	Power Dissipation (mW)
1	0.2	280	29
4	1.2	125	29
7	2.2	81	28
10	3	59	28

There is clearly a trade off between gain and bandwidth in selecting R_f.

We then look at the effect of the collector resistance, R_c on the circuit performance in a similar way in the following table. It is apparent that although an increase in R_c improves the circuit performance, the improvement diminishes as R_c approaches R_f. This behavior is due to the effect of R_c on voltage gain, as seen in Eq. 2.22. Thus R_c effects the values of R_{f1} and $C_{\mu 1}$, and the bandwidth. In our circuit, a more ideal value for R_c would have been 7 kΩ.

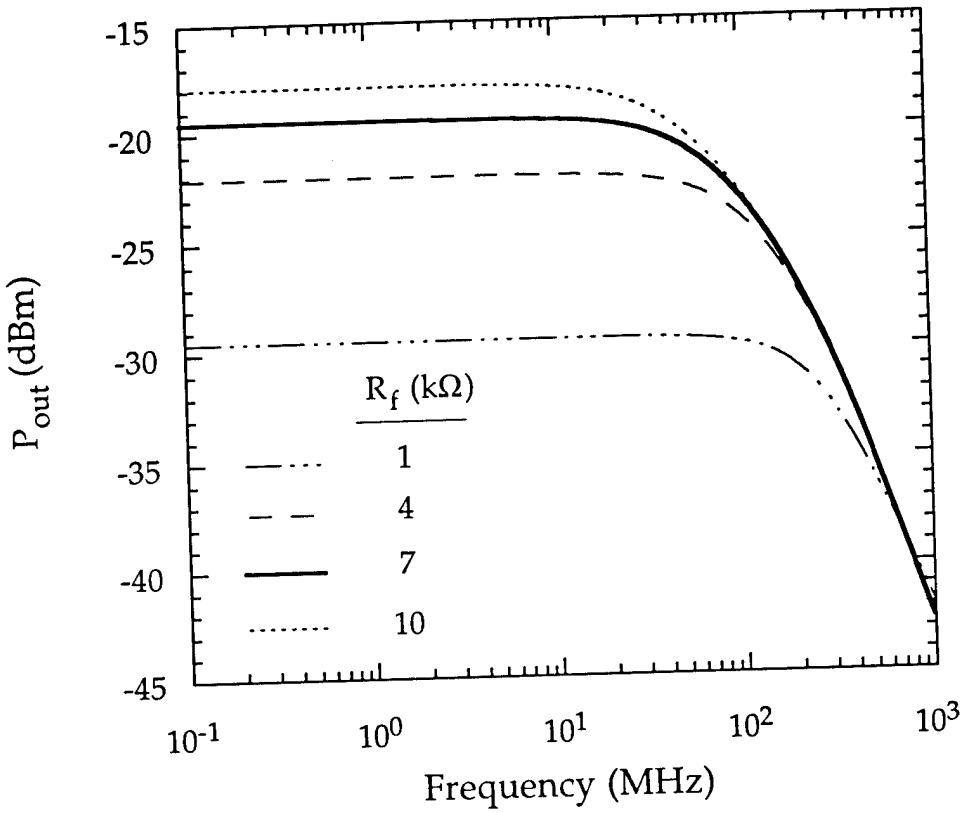

Fig. 2.10: The bandwidth of the smart pixel for different values of feedback resistor, R_f, obtained from SPICE analysis.

R_c	Gain	Bandwidth (MHz)	Power Dissipation (mW)
500	1.3	66	40
1 kΩ	1.8	72	33
2 kΩ	2.2	83	29
4 kΩ	2.4	9 1	25
7 kΩ	3.8	91	24
10 kΩ	2.4	91	23

The effect of front end emitter resistance is given below:

R_e (Ω)	Gain	Bandwidth (MHz)	Power Dissipation (mW)
0	2.6	95	27
100	2.4	85	27.8
200	2.2	81	28
400	2.0	78	29

Lower values of R_e result in better circuit performance. However, we chose the value of 200 Ω in order to pull up the front end output voltage closer to the base-emitter junction voltage of Q_3 in the differential pair, and to provide an additional mechanism for negative feedback.

Finally, we consider the resistance at the emitter of the differential pair:

R_{EE} (Ω)	Gain	Bandwidth (MHz)	Power Dissipation (mW)
50	1.5	83	52
150	2.2	81	28
300	2.4	80	18

Our choice of 150 Ω for this resistor is again a suitable medium in the values.

The DC supplies used in biasing the circuit can also effect the performance. We first consider the effect of the main bias supply, V_{cc}:

V_{cc} (V)	Gain	Bandwidth (MHz)	Power (mW)
2.0	2.1	78	25.5
3.0	2.3	81	28
4.0	2.4	83	31.5

Thus, although higher supply voltage results in higher gain and bandwidth, it increases the dissipated power.

It was mentioned earlier that the current swing at the output can be improved by applying a negative bias to the emitter resistor of the differential pair (V_E). The effect of this voltage is summarized as follows.

V_E (V)	Gain	Power Dissipation (mW)
0	1.0	6.0
-0.5	2.0	16.2
-1.0	2.2	28.6
-1.5	2.4	43.0

In our circuit, the base of Q_3 in the differential pair was fixed at 0.85, which is in the midrange of the front end output swing. This voltage is supplied by an off-chip power supply. Let us now consider the effect of this voltage on circuit performance.

V_{b3} (V)	Gain	Power (mW)
0.75	2.1	27.5
0.85	2.2	28
0.95	2.3	29.5

The effect of this voltage is rather weak.

We observed how each component parameter (or bias) can effect the circuit performance. There is always a trade off between different figures of merit. The exact choice of the circuit component value is dependent on the specific application, and needs to be optimized for the required functionality.

2.3.3 Section Summary

We summarize the performance of the smart pixel by considering the three factors which were earlier referred to as the pixel figures of merit. In preceding discussions, we found the large signal gain of the circuit to be ~3. We also obtained the value of 81 MHz for the circuit bandwidth. The power dissipation in the circuit can be found by $P=(I_{c1}+I_{c2}+I_{c3})V_{cc}+V_{EE}I_{REE}$. Using Fig. 2.3 and 2.4 we find that the receiver dissipated power is 24 mW. The power dissipated by the laser is the product of the voltage drop across the laser, V_L and the laser current: $P_L = I_L V_L$=37 mW. This power can be reduced by using lasers with lower threshold currents. The total pixel power dissipation of ~60 mW, therefore, limits the packing density to ~20 pixels/cm^2 (assuming 1 W/cm^2 power dissipation which is the limit for passive cooling).

2.4 Discrete Device Requirements

In this section, we study the relation between the performance of the active and passive circuit components and their effect on the total circuit performance. We start with the p-i-n photodetector. The dark current of the photodetector influences the system noise. Secondly, the quantum efficiency of the p-i-n is important in determining the gain of the pixel, seen in Eq. 2.21.

The HBT gain also impacts pixel performance. Larger values of β, give rise to higher base-emitter internal resistance, $r_\pi=\beta/g_m$, and hence limit the bandwidth. On the other hand, as shown in Eq. 2.15 large β can assure performance that is independent of specific device parameters, and hence higher yield. An increase in β reduces the quiescent base current for a fixed collector current, thus reducing the shot noise. Further effects of the HBT

characteristic is through C_{bc}, which determines the circuit bandwidth and needs to be minimized.

We have simulated the frequency response of the pixel for different values of base-collector junction capacitance, referred to C_μ or C_{bc}. The results are plotted in Fig. 2.11, and summarized below. It can be seen that decreasing this capacitance, results in significant bandwidth improvements.

Base-Collector junction capacitance, C_{bc} (fF)	Bandwidth (MHz)
100	200
200	120
300	81
400	65

The base resistance of HBT's is generally low, due to the high doping in this region. However, if the contact resistance is high, the overall base resistance, defined as the sum of the sheet and contact resistances, will no longer be negligible. Below, we have calculated the effect of this resistance on circuit bandwidth. The base resistance is especially important for thin base HBT's, where both sheet and contact resistances tend to be high.

Base resistance (kΩ)	Gain	Bandwidth (MHz)	Power Dissipation (mW)
1.0	2.2	81	28.0
3.0	2	66	27.7
5.0	1.7	53	27.4

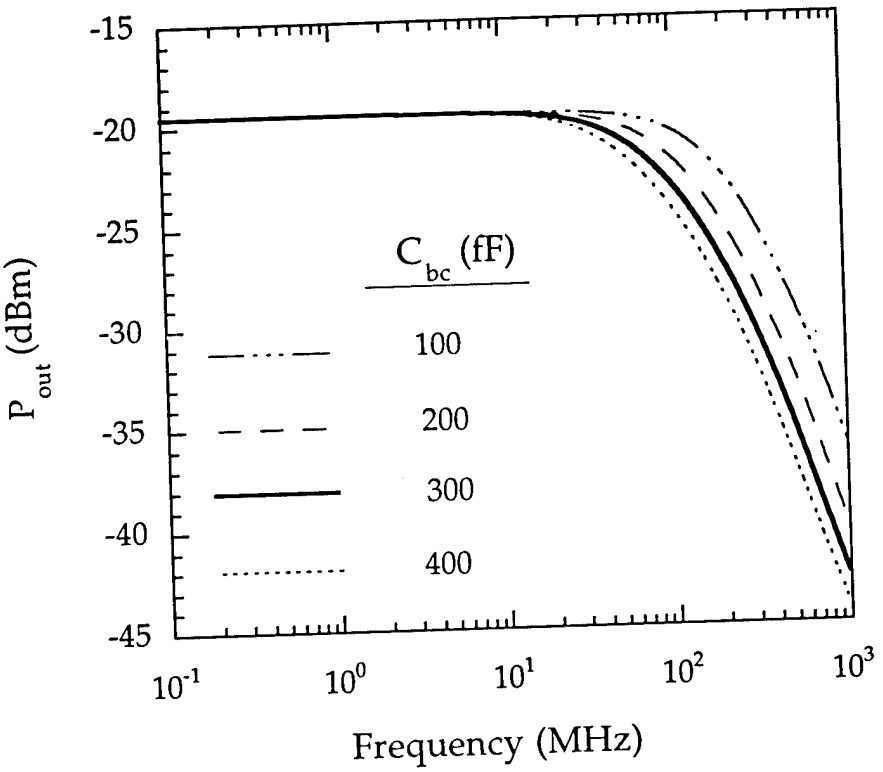

Fig. 2.11: Bandwidth of the smart pixel for different values of the base-collector junction capacitance, C_{bc} (or $C\mu$) from SPICE.

The laser parameters most relevant to the circuit performance include threshold current, slope efficiency, and modulation speed. Threshold current needs to be minimized to reduce the prebias current and its associated power. The following table shows the effect of the laser slope efficiency on the pixel gain. The three values of η_d considered here correspond to the worst, average and best slope efficiencies obtained for our FCSEL's at 1.3 μm.

Laser Slope Efficiency (η_d)	Gain
10% (worst)	1.3
17% (average)	2.2
30% (best)	4.0

The bandwidth of the laser can also be a potential limitation to pixel speed of response. Generally, however, the modulation speed of the laser is sufficiently high (~ 1 GHz) such that it is not the limiting factor.

The performance of the smart pixel is largely controlled by the resistor values, since it is generally easier to control the yield in resistor fabrication compared to the gain or other characteristics of transistors. Therefore, it is of utmost importance that the resistor values be reproducible. We performed simulations to predict the circuit performance for a variation of the resistor values by 20%. In the worst case, when all resistors vary in the direction of degrading the performance, pixel operation will degrade by $\leq$10%.

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Chapter 3

Material Growth and Fabrication of the Smart Pixel

3.1 Introduction

In this chapter, the growth technique, wafer structure, and fabrication steps for the smart pixel are discussed. The pixel structure was fabricated in the InP/InGaAsP material system to ensure compatibility with long wavelength applications[1,2]. The material quality is of great importance for this design, as it determines surface and bulk trap densities. These parameters have direct influence over the performance of the smart pixel circuit elements[3]. In section 3.2 material growth and characterization of the wafer are presented. That is followed in section 3.3 by a step-by-step processing sequence of the pixel. Section 3.4 contains the details of the folded cavity surface emitting laser (FCSEL) fabrication process. In section 3.5, design of the photolithography mask layout will be discussed.

3.2 Growth of the pixel structure

3.2.1 Growth technique

The methods commonly used to grow InP-based materials include metal organic chemical vapor deposition (MOCVD), liquid phase epitaxy (LPE), and molecular beam epitaxy (MBE). Compared with the other crystal growth techniques, MBE provides the greatest precision in thickness control

and abruptness of growth interfaces[4]. In MBE, growth is accomplished by vaporizing elemental sources of group III and V atoms in a high-vacuum chamber[5]. The molecular species are collimated into beams which are then coincident on the crystalline substrate that acts as a site for epitaxial growth by adhesion of the incident atoms. The composition of the resulting layer is a function of the fluxes of the various beams as well as the probability that a given constituent species will stick once it hits the substrate[6].

Elemental source MBE using solid Phosphorus (P) and Arsenic (As) as group V sources is not well-suited for growing P containing compounds, such as InP-based materials. The reasons are three-fold. First, fast consumption of P due to its high vapor pressure results in the need for frequent recharging of the source by opening the growth chamber, which is undesirable. The alternative is using large effusion cells, which is also problematic due to poor thermal conductivity of the solid in the cell, and hence difficulty in temperature control[3]. Secondly, the high vapor pressure of P makes it difficult to control the beam flux[7]. Finally, species generated from a solid P source consist principally of the tetramer form of this element, P_4, which results in inferior material quality[8]. Gas source molecular beam epitaxy (GSMBE) using elemental group III and gaseous group V sources is particularly suitable for growing InP based structures which require good abruptness and thickness control[3] .

The smart pixel wafer in this work was grown using GSMBE, where the gases PH_3 and AsH_3 were used to supply group V, and elemental Indium and Gallium sources were used for group III materials. In this growth, Si and Be were used as the n and p type dopants, respectively. The growth conditions are presented in detail elsewhere[9].

3.2.2 Epitaxial structure of the pixel

The smart pixel structure consists of eight monolithically integrated devices and a surface bonded folded cavity surface emitting laser (FCSEL). The integrated devices include: a p-i-n photodiode, three heterojunction bipolar transistors (HBT's), two semi-conductor slab resistors (used in the 1-10 kΩ range), and two Titanium (Ti) thin film resistors (used in the 100-200 Ω range). Therefore, it is necessary for the growth and processing steps to be compatible with all of these devices. The HBT and the p-i-n devices have mesa structures, with HBT's having emitter-up configuration. Hence, there is no need for dopant diffusion, as the impurities can be incorporated in the layers during growth. The HBT/p-i-n wafer was grown on (100) semi-insulating InP. The epitaxial structure of the smart pixel is presented in Table 3.1.

The highly doped InGaAs layers in the emitter cap and the subcollector contact regions are included to provide low contact resistance. As mentioned in Ch. 2, two main advantages of HBT's for high speed applications stems from the freedom to lower the emitter doping and increase the base doping without a loss of current gain. Here, the emitter doping was chosen to be low to reduce the capacitance of the forward biased base-emitter junction (C_{be}). The doping of the base was chosen high to also reduce C_{be}, and the base resistance (r_{bb}), in order to improve bandwidth of the pixel. The abruptness of the base-emitter junction results in a spike in the conduction band, which may cause non-equilibrium near-ballistic transport in the base[10]. The collector layer is undoped in order to reduce the base-collector junction capacitance (C_{bc}). Lowering this parameter results

Table 3.1

Epitaxial Structure of the Smart Pixel Wafer

#	Device Layer	Material	Thickness (Å)	Doping (cm^{-3})
1	Emitter cap	n^+ InGaAs (Si)	2000	$3x10^{18}$
2	Emitter	n InP (Si)	2000	$1x10^{17}$
3	Base	p^+ InGaAs (Be)	800	$1x10^{19}$
4	Collector	undoped InGaAs	3000	------
5	Etch stop	n^+ InP (Si)	500	$5x10^{18}$
6	Subcollector	n^+ InGaAs (Si)	2000	$5x10^{18}$
7	p-photodiode	p^+ InP (Be)	3000	$1x10^{18}$
8	i-photodiode	undoped InGaAs	$1.5x10^4$	------
9	n-photodiode	n InP (Si)	1500	$1.5x10^{17}$
10	Substrate	Semi-insulating InP	------	------

insignificant improvements in the pixel bandwidth as seen in Ch. 2. The etch stop between collector and sub-collector was necessary to define the base-collector mesa. The doping of this layer was chosen high, to reduce the series resistance of this wide band gap layer. The band diagram for the abrupt InP/InGaAs HBT's is shown in Fig. 3.1.

The doping of the p layer of the p-i-n photodiode was chosen so as to reduce contact resistance. In p-i-n photodiodes, there exists a trade-off between sensitivity and bandwidth in selecting the thickness of the i-layer. A thicker intrinsic layer enhances the absorption, thus increasing the detector quantum efficiency and sensitivity. However, the device transit time is longer for thicker layers, hence reducing the device bandwidth. Furthermore, in order to maximize the detector efficiency, the i-layer needs to be fully depleted. The thickness of this layer, therefore, must be selected such that the required voltage is feasible from the point of view of pixel operation. We chose the thickness of the i-layer to best satisfy the sensitivity/bandwidth considerations, and such that full depletion would be accomplished by applying a voltage of 1 V across the device.

The n-layer of the p-i-n also forms the layer from which the semiconductor slab resistors are fabricated. Hence, the doping and thickness of this layer were designed so as to optimize its dual functionality.

In order to determine the quality of the epitaxial growth by measuring layer thicknesses and doping, we employed electrochemical capacitance-voltage (CV) profiling techniques using a Bio-Rad PN4300PC profiler. This method does not suffer from the main constraint of conventional CV measurement, i.e. the profile depth, which is limited by the reverse breakdown voltage of the Schottky contact that is formed for the

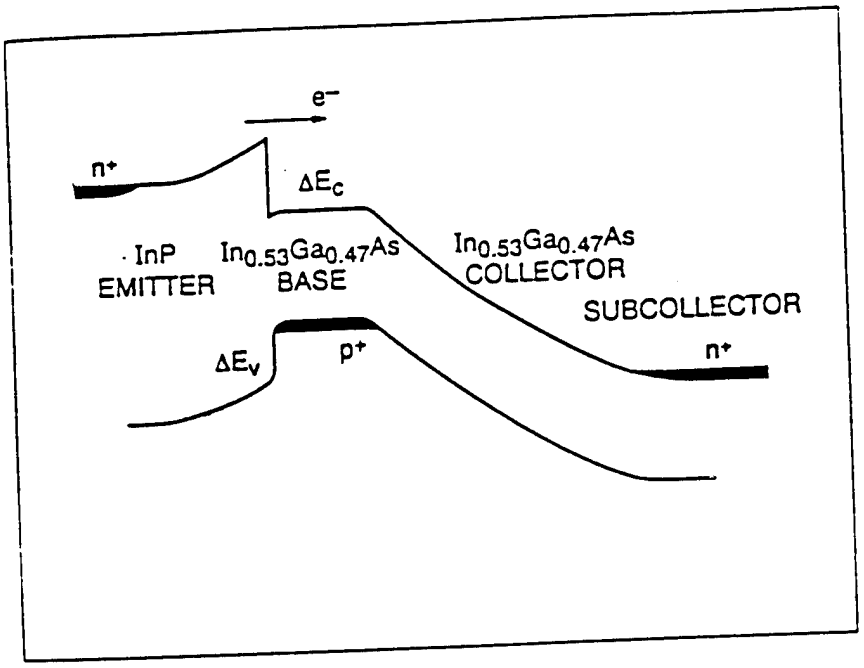


Fig. 3.1: Energy band diagram of the InP/InGaAs HBT's. For this heterojunction, ΔE_c=0.25 eV, and ΔE_v=0.34 eV (Ref. [11]).

measurement. Electrochemical techniques enable profiling the thickness and doping of the sample regardless of the thickness or majority carrier type, as the sample is electrochemically etched with adjustable increments, and a CV data point is obtained at each step. This destructive profiling technique measures the concentration of dopants which are electrically active, and not their chemical concentration. The electrolyte used for the electrochemical etching process was 10 cc Ethylene Diamene in 500 cc of 0.2 molar EDTA solution in DI water. Since the etching is done by removing the holes from the surface, the sample is always held under positive bias and the electrolyte under negative bias, i.e. forward biasing a p-type sample versus reverse biasing an n-type. Furthermore, in the case of n-type layers, due to the deficiency of holes, light is used to generate minority carriers which contribute to the etch current. The doping and thickness profile of a typical pixel wafer is shown in Fig. 3.2. It can be seen that the intrinsic doping in the collector and the i-layer of the p-i-n are higher than the expected value by about a factor of 3.

3.3 Fabrication of the integrated devices

A crucial fabrication issue of this pixel is the required compatibility of the processing sequence for the four different device types integrated in the circuit, and the FCSEL which was later surface bonded. Hence, each component must remain intact throughout the processing of the other components. The pixel fabrication includes 10 photolithographical steps. The processes employed were wet etching, annealing, surface passivation using polyimide, curing and patterning the polyimide film, metal deposition for resistors, contacts and interconnects, and surface bonding the laser. The

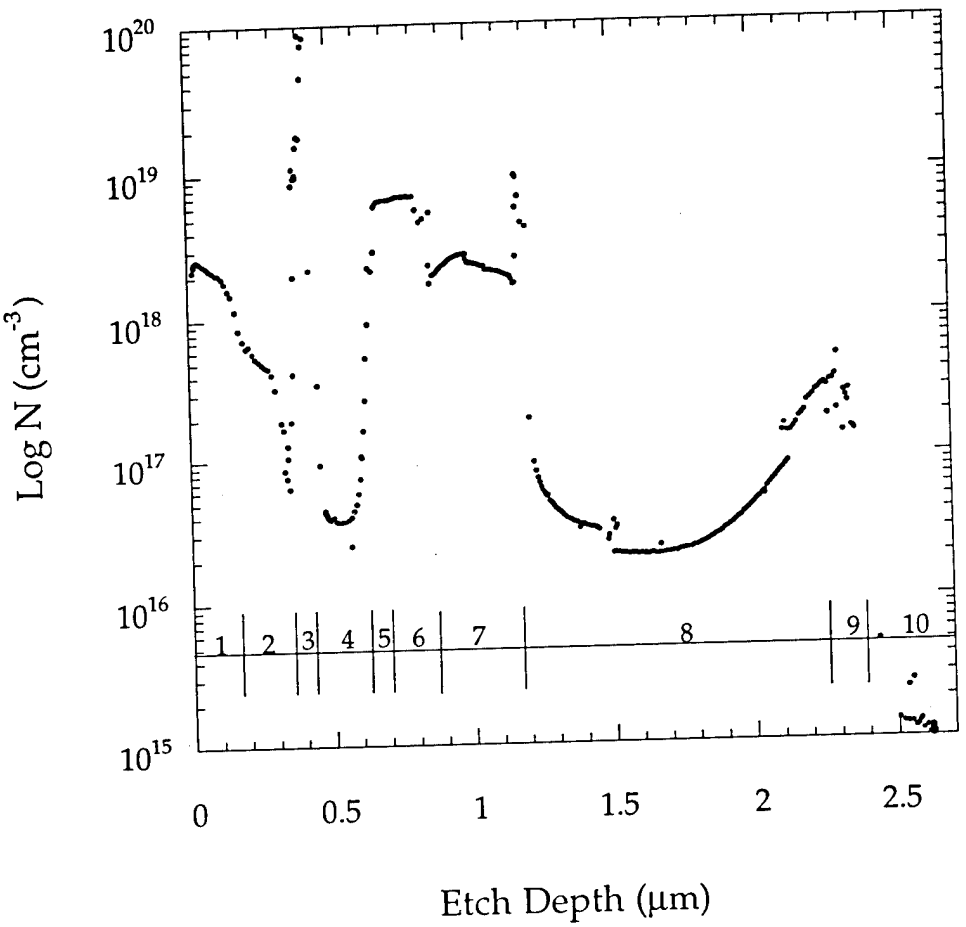


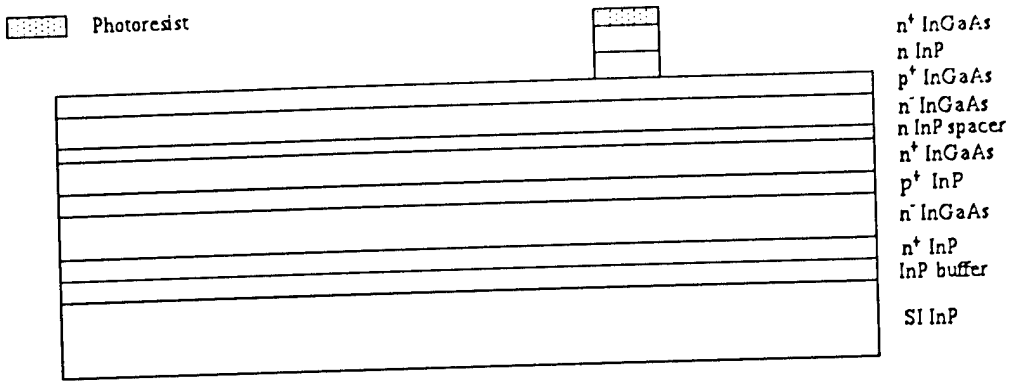
Fig. 3.2: The epitaxial structure of the smart pixel determined by electrochemical C-V measurements. Layer numbers correspond to those in Table 3.1.

order in which the processing was carried out is depicted in Fig. 3.3. The complete details of the process sequence are presented in Appendix C.

The pixel fabrication begins with cleaning the wafer. The epitaxial wafer was mounted on the MBE block using Indium, which was later removed by wax-mounting the wafer followed by lapping and thinning. The sample was then cleaned in boiling TCE for 5 minutes, and rinsed thoroughly with Acetone and Iso-Propanol. In cases where the wafer was stored in the desiccator for some time, it was further cleaned using a 1:10 solution of saturated Tergitol in de-ionized (DI) water prior to processing.

The next step was photolithography for defining the devices. Throughout the fabrication steps, we avoided exposing the sample to plasma whenever possible. The reason was our findings as well as reports by others[12] that the exposure to high energy, or high temperature plasma (for dry-etching or growth of dielectric films) causes damage on the sample surface. The resultant large surface defect density gives rise to high leakage current for HBT's and high dark current for p-i-n diodes. This damage was noticeably decreased by reducing the plasma power during dry etching, and entirely eliminated by following the dry etch with wet etching. The lowering of the temperature in growth of dielectric films, however, was not a viable option. The reason is the poor quality of plasma-enhanced dielectric films deposited at low temperatures[13]. Thus, we used material selective wet etching to form the mesas, employing positive photoresist as the etch mask. The etchants were a 5:1:5 Citric acid (50%):H_2O_2:H_2O solution for etching $In_{0.53}Ga_{0.47}As$ and a 3:1:3 solution of HCl:H_3PO_4:H_2O for etching the InP. Another possible etchant was a 1:5:0.1 solution of HBr:H_2O:H_2O_2, which would etch both InP

1. Emitter mesa etch



2. Base, subcollector and spacer mesa etch
3. Collector mesa etch

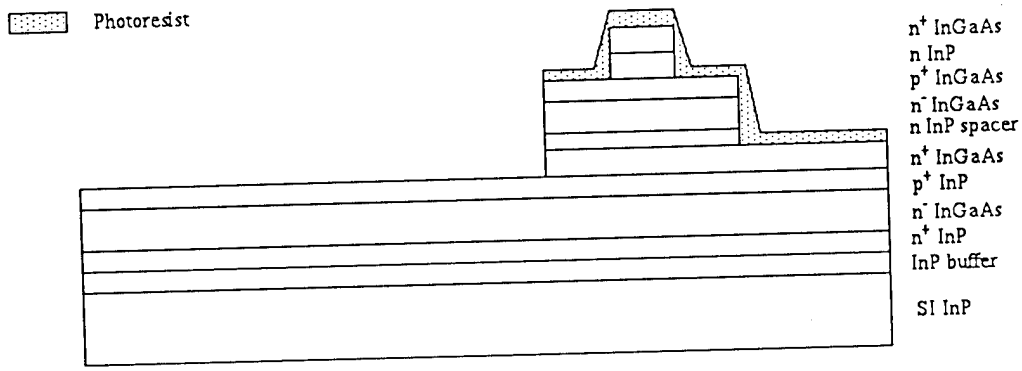
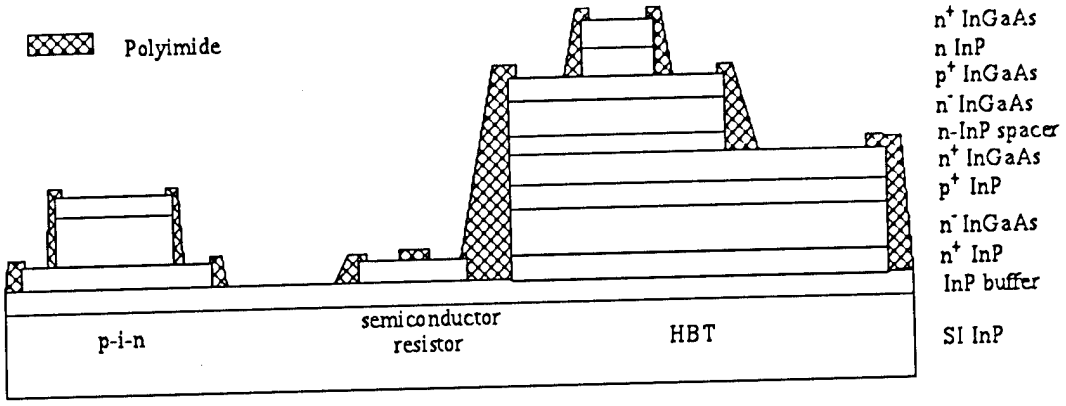


Fig. 3.3: Processing sequence for the smart pixel.

6. Polyimide deposited, cured and patterned



7. Metal thin film resistor deposition
8. P-type contact metal deposition
9. N-type contact metal deposition

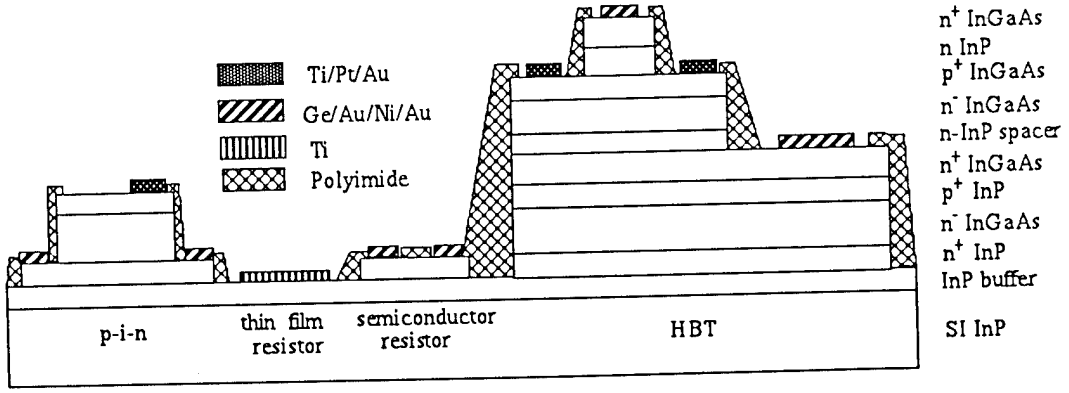


Fig. 3.3 (continued)

10. Interconnect metal deposition
11. Surface bonding the FCSEL

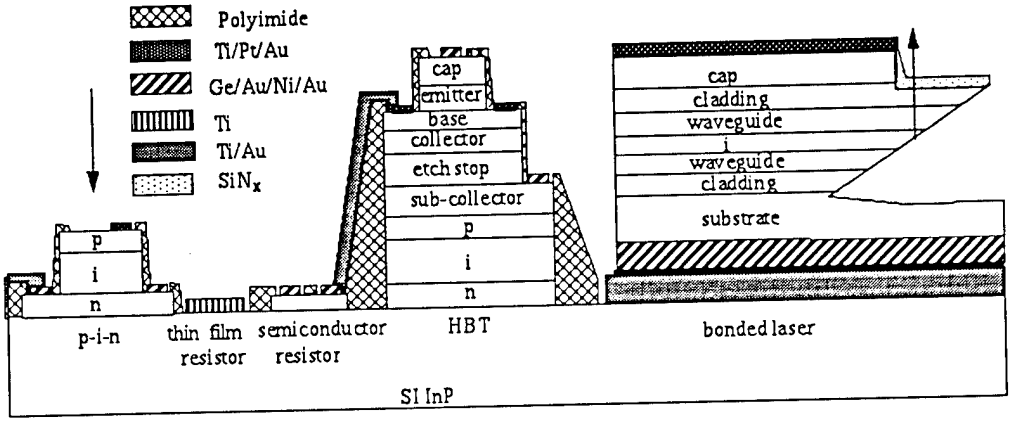


Fig. 3.3 (continued) The schematic profile of the complete smart pixel.

and InGaAs, however, it also formed notches next to the mesa side walls, which were as high as 50% of the mesa height. Table 3.2 includes etchants for different layers, their material selectivity, and etch rates as measured in this work.

After etching the HBT mesa, the p-i-n mesa was defined by etching the p and i layers, while protecting the HBT mesa with photoresist. In the next step, the n layer of the p-i-n was etched, also forming the semiconductor resistor slabs. The resistivity of this layer was 10^{-2} Ω-cm.

A challenging aspect of processing different types of devices monolithically, was choosing a surface passivation method compatible with all devices. Passivation refers to the removal or neutralization of undesired surface states. Passivation has also been used to describe processes where the surface is encapsulated by a film such that the surface states are reduced or eliminated by the presence of the passivating layer interface. Unpassivated p-i-n surfaces show large dark currents. Furthermore, passivation of HBT sidewalls is important in providing electrical isolation, as well as device protection during packaging. The passivation film also needs to provide a smooth profile for the mesas, assuring continuity of the interconnect metal along the mesa edges.

Compared to GaAs/AlGaAs HBT's, InP-based devices have a lower surface recombination velocity, thus, a lower surface leakage current[14]. This leakage current is undesirable, in that it reduces the current gain (β) at low collector current (I_c) levels. Several laboratories[12,15] have observed HBT Gummel plots showing significant β down to low I_c without surface passivation. However, on the same wafer and with the same process steps, we also observed HBT's with high surface leakage. In these devices, surface

Table 3.2

Wet Chemical Etch Characteristics

Etchant	Etched	Not Etched	Etch Rate	Comment
$3HCl:H_3PO_4:3H_2O$	InP	InGaAs	400 Å/min	(a,b)
$HCl:H_3PO_4$	InP	InGaAs	1000 Å/s !	(a,b,c)
$5(50\%\ Citric):H_2O_2:5H_2O$	InGaAs	InP	400 Å/min	(d)
$HBr:5H_2O:0.1H_2O_2$	InP InGaAs	---	200 Å/min	(e)

(a) Etch pits form when etching InP substrate

(b) Undercut

(c) The etch rate is too fast, bubbles form and create non-uniformities

(d) No undercut

(e) Notches form next to the etched mesa side walls

passivation reduced the leakage current, resulting in better current gain at low I_c levels. Passivation also significantly lowered the p-i-n dark current. Further, it did not degrade the characteristics of the already low-leakage devices.

In order to formulate a general process sequence, we used polyimide for the passivation of all samples. Polyimide (Probimide 285, OCG Microelectronics Materials, Inc.) consists of polyamic acids with structures that have both rigid and flexible elements. It is essential to cure polyimide under well-monitored conditions to achieve full cross-linking, thus to ensure good mechanical performance as well as electrical isolation.

Here, we present the optimum passivation sequence found: Prior to polyimide spin-on, the wafer was annealed in a rapid thermal annealer (RTA, AGA Associates) at 365 °C for 90 seconds in a non-oxidizing atmosphere (9:1 N_2:H_2). It was then treated in a BHF (10:1 H_2O:HF) solution for 5 minutes. Next, a 6000 Å thick polyimide layer was spun on, and was fully cured in a N_2 purged oven at 300 °C for 30 minutes. We then deposited 1000 Å of electron beam evaporated SiO_x to act as the etch mask for patterning the polyimide. Patterning was done in order to open windows in the polyimide for metal deposition. The SiO_x was etched using BHF, and polyimide was patterned using O_2 reactive ion etching (100 W, 100 mTorr). The SiO_x was then stripped using BHF. This process has been previously published, though the passivation mechanism was not well understood at the time[16].

In the passivation process, it is apparent that both the anneal and the BHF dip are required to achieve the best results. For InP, InGaAs, and also GaAs, surface states are thought to be related to stoichiometric deficiencies,

i.e. to excess group III or group V elements misplaced from their normal positions[9]. Therefore, we expect to have an excess of As and P, or In and Ga on the side-walls of the HBT and the p-i-n mesas. It has been shown that surface treatments of III-V materials with gaseous nitrogen compounds at about 300°C can be used for removing native oxides (such as $InPO_4$ or In_2O_3) and excess group V elements[13,17]. In our process, the exposure to N_2 at 365°C can function similarly, thus removing the weakly bonded oxygen atoms and stabilizing the one-monolayer oxide, i.e. it turns the initial oxide into a thinner, well-defined, and more stable oxide. This oxide layer is then removed by the BHF treatment, which is well known for this property. The BHF solution may also react with the group III dangling bonds on the surface to form InF_3, and possibly GaF_3[18]. Furthermore, this solution has been shown to remove defects in the surface damaged layer which can result from plasma exposure[13].

Among the most stable passivation methods for III-V compounds, is deposition of a semi-insulating, lattice-matched layer on the surface[19]. It is well known that H_2 annealing will accomplish this goal by passivating the surface dopants[20]. In addition, annealing is known to drive H_2 into the sample bulk, hence extending its dopant passivation beyond the first few surface monolayers[21]. Therefore, the annealing in the presence of H_2 in our case, may help passivate the surface further.

Thus, it follows that both the annealing in the presence of H_2/N_2 and BHF dip are required for best passivation results: The anneal effects the surface native oxide, removes excess group V atoms, and H-passivates the surface, while BHF removes the oxide or damaged layers, and binds to the group III states.

The next process step was metal deposition for thin film resistors. Initially, NiCr was used for this purpose. The problem with this alloy was that at thicknesses beyond 1500 Å, the film would demonstrate poor adhesion to the substrate and peel off. Therefore, we used Ti for the thin film resistors. The metal thickness used was 2200 Å, resulting in the sheet resistivity of 5 Ω/square. At this thickness, a 5% variation in metal thickness gave rise to a 10% change in resistivity. The Ti resistors showed suitable temperature stability throughout the processing steps, and their values remained unchanged during the measurement.

The next step was metal deposition for the base contact. Application of the commonly used p-type contact metal, Zn/Au[22], was not an option for us, as it would result in shorted base/emitter junctions. This effect was attributed to the diffusion length of Zn being longer than the base width, causing it to punch through the 800 Å base[23]. Therefore, we chose Ti/Pt/Au for p-contact metal. We found that although using this contact metal for both the p and the n layers was possible, it resulted in too large a contact resistance to the n-type layers. This was especially problematic in the case of the semiconductor feedback resistor, whose total resistance would be large enough to pull the output of the front end (Q_1) into saturation for small input power levels. Hence, we used Ti/Pt/Au at 300/400/1000 Å for p-type contacts and Ni/Au/Ge/Au at 250/450/215/1000 Å for n-type contacts. We then deposited pad and interconnect metal using Ti/Au at 250/2000 Å thickness.

3.4 Laser Fabrication

The 1.3 μm wavelength, strained multiple quantum well (MQW) InGaAsP/InP FCSEL has a 45° angled facet, a cleaved back facet, and a 4 μm wide, 600 μm long ridge waveguide[24]. The structure was grown by GSMBE on an n^+ (100) InP substrate (doped with S at 3.8×10^{18} cm^{-3}). The layer structure was grown as follows: A 1 μm thick, lightly doped (with Si at 2×10^{17} cm^{-3}) InP lower cladding layer, a 1200 Å thick, undoped InGaAsP lower waveguide layer which had a bandgap cutoff wavelength of λ_g=1.15 μm, the active region consisting of five compressively strained InGaAsP quantum wells with 105 Å wide barriers (λ_g=1.15 μm) and 67 Å wide wells (λ_g=1.4 μm), a 1200 Å thick, undoped InGaAsP upper waveguide layer with λ_g=1.15 μm, a 1.2 μm thick, (Be-doped at $2\text{-}5 \times 10^{17}$ cm^{-3}) InP upper cladding layer and an 800 Å thick, p^+ InGaAs top contact layer (Be-doped at 2×10^{18}). The angle etching was done in a reactive ion etching (RIE) system using a 5:1 CH_4:H_2 mixture. The contact metals were Ti/Pt/Au (200 Å/500 Å/4000 Å), and Ge/Au/Ni/Au (270 Å/450 Å/215 Å/1200 Å) for the p and n-type contacts, respectively. A schematic of the FCSEL profile is given in Fig. 3.4.

Surface bonding of the laser n-contact to a metal pad immediately adjacent to the pixel employed silver epoxy to achieve good electrical and thermal contact. The bond was fully cured at 140°C on a hot plate for 10 minutes. The p-contact was then wire-bonded onto a pad on the pixel or probed during the measurements.

3.5 Device geometry and mask layout

The dimension of the pixel was 600x600 $(\mu m)^2$. The main factor in determining the pixel size was the length of the laser. In addition to the 2x2

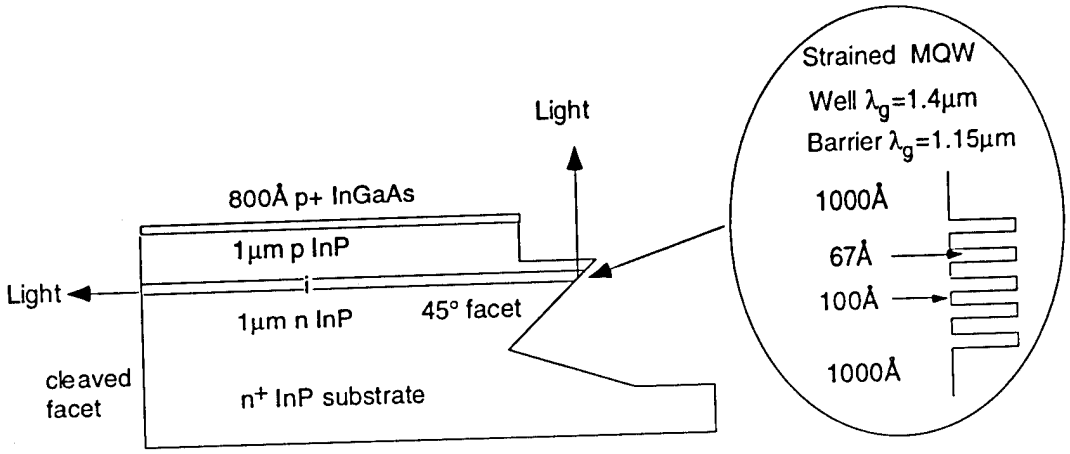


Fig. 3.4: The schematic profile of the FCSEL.

arrays of the smart pixel, the mask also contained many test structures for different parts of the circuit. These included the front end, the differential amplifier (with and without bonding pad for the laser), and individual devices, such as HBT's, p-i-n's, metal and semiconductor resistors, and tuning fork patterns for testing the resolution of lithography steps.

The base-emitter junction areas of the HBT's were (7x11) $(\mu m)^2$, those of the base-collector junctions were (15x31) $(\mu m)^2$, and the p-i-n diameter was 40 μm. The diameter and the circular shape of the p-i-n diode were designed to be compatible for use with a multimode fiber to carry the input beam. Furthermore, a circular shape would avoid the existence of sharp corners that can give rise to high field regions and increase the dark current. Photomicrographs of the completed smart pixel circuit are presented in Figs. 3.5 (a), (b). The layout was done in AutoCAD, version 10. The complete layout for the mask set is included in Appendix D.

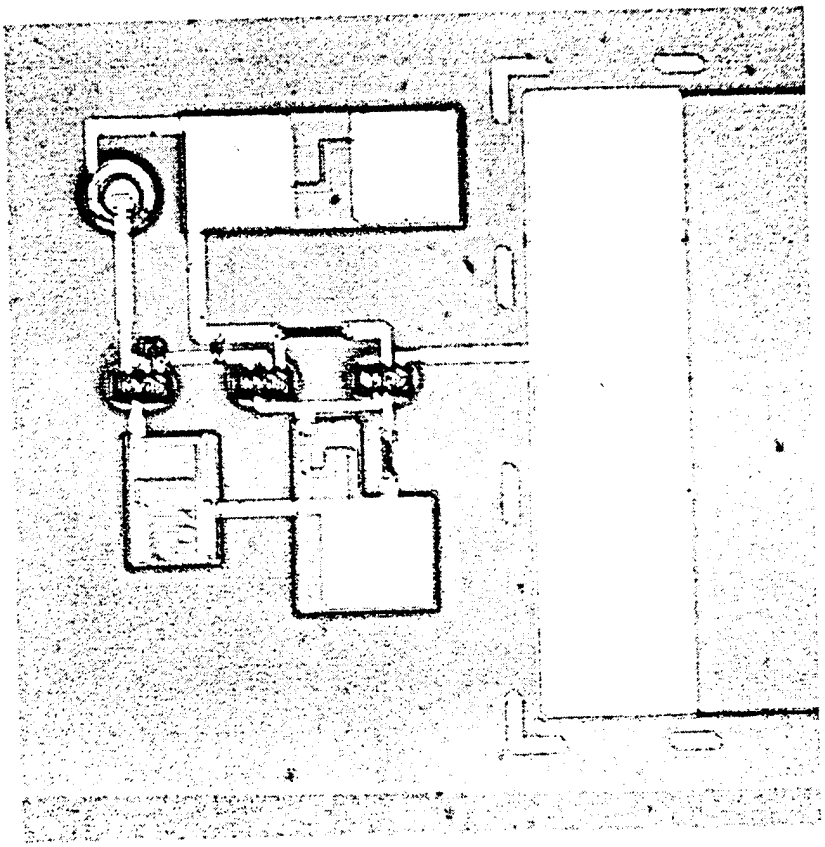


Fig. 3.5 (a): Photomicrograph of the integrated part of the smart pixel.

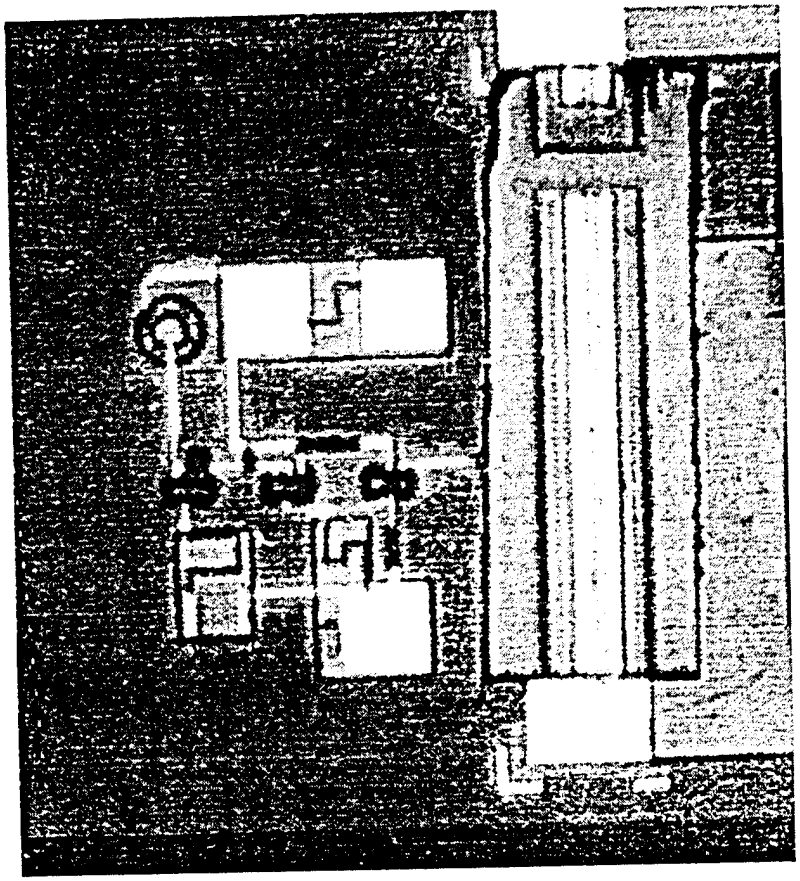


Fig. 3.5 (b): Photomicrograph of the completed smart pixel, including the surface mounted laser.

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Chapter 4

Experimental results on the smart pixel

4.1 Introduction

In this chapter, we present the results obtained from measurements on the hybrid/integrated smart pixel. The smart pixel circuit consists of a p-i-n/HBT transimpedance amplifier at the front end, followed by an HBT differential pair with a surface bonded FCSEL. Except for the FCSEL, all the other components are monolithically integrated. We demonstrate that this pixel is capable of optical gain and cascadability for bit rates of up to 100 Mb/s. The main achievement of this circuit is the very low switching energy of 14 fJ as a stand alone receiver. With gain and cascadability, the switching energy is 30 fJ. This is the lowest switching energy obtained to date for smart pixel transceiver technologies.

This chapter is organized as follows. In section 4.2 results on discrete pixel components will be discussed, followed in section 4.3 by the measurement results on the operation of the full pixel. Section 4.4 compares the switching energies for different smart pixel technologies. Section 4.5 includes measurement results on the temperature dependence of the smart pixel components. The implications of this dependence for the overall pixel performance will be discussed in section 4.6.

4.2 Performance of discrete smart pixel components

4.2.1 The p-i-n photodiode

The p-i-n photodiode characteristics which impact the pixel performance are dark current, bandwidth, and voltage dissipation. Fig. 4.1 shows the dark current at a reverse bias of 0-3 V at room temperature. The dark current at 1 V is about 20 nA for an average device, with dark currents as low as 2 nA for the best p-i-n photodiodes. The dark current increases sharply up to 0.5 V, then levels off. This indicates that in order to fully deplete the photodiode for best efficiency, a voltage drop of at least 0.5 volts is required across the device. Hence, the circuit bias supply needs to be selected such that it provides the required voltage for optimum operation of the p-i-n photodiode and the HBT's.

We have measured the p-i-n photodiode frequency response using an HP 8703 optoelectronic network analyzer as shown in Fig. 4.2. This instrument includes a modulated DFB laser as the internal source, and an electrical response analyzer. The measured 3-dB point is 7.5 GHz. This agrees well with the calculated bandwidth of 8 GHz, obtained from calculating the device RC delay. The quantum efficiency for typical p-i-n photodiodes was about 65% at wavelength of 1.3 μm.

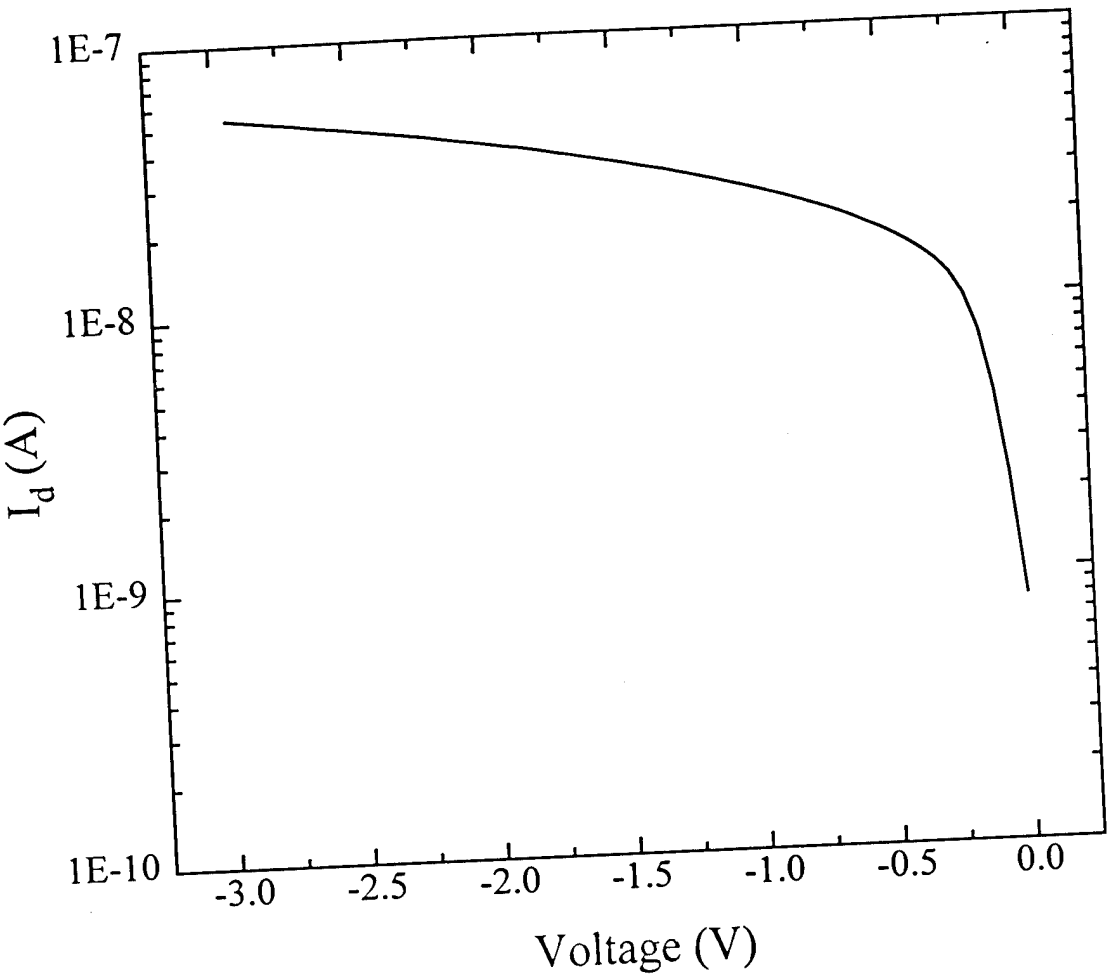

Fig. 4.1: Dark current characteristics for an "average" p-i-n photodiode.

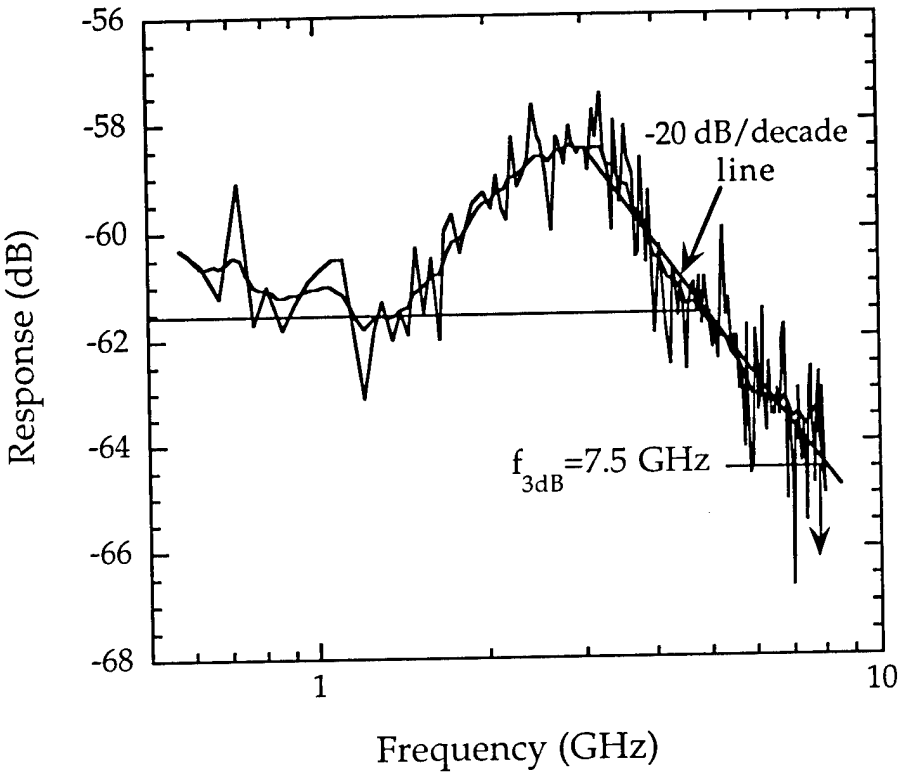

Fig. 4.2: The frequency response of a p-i-n photodiode.

4.2.2 HBT characteristics

The electronic processing elements of the smart pixel consist of three HBT's. In Fig. 4.3 we show the common emitter DC characteristics of a typical smart pixel HBT. For a collector current of 1 mA, the current gain was consistently in the range of 100-400. This, to our knowledge, is the best value of current gain obtained to date for integrated InP/InGaAs HBT's[1-4]. The Gummel plot of collector and base currents (I_c and I_b) vs. base-emitter voltage is shown in Fig. 4.4. The remarkable characteristic of this plot is parallel current curves, indicating significant current gain, β, down to sub-nano-ampere collector currents. This fact, taken together with the high current gain in the mA range, is advantageous for low power operation of the smart pixel. It was shown in Ch. 2 that a current gain >100 is required for good pixel performance. Furthermore, large β at low collector currents allow pixel operation in this regime without a loss of functionality. This will result in an improvement of receiver sensitivity and switching energy. The HBT 3 dB bandwidth is estimated to be 40 MHz. The limiting factors in determining the bandwidth are the base-collector junction capacitance, C_{bc}, base-emitter junction capacitance, C_π, and the dynamic base-emitter resistance, r_π (or r_{be}). Therefore, the HBT 3 dB bandwidth can be calculated as: $\omega=[r_\pi(C_{bc}+C_\pi)]^{-1}$. The parameter values are the same as in Table 2.3.

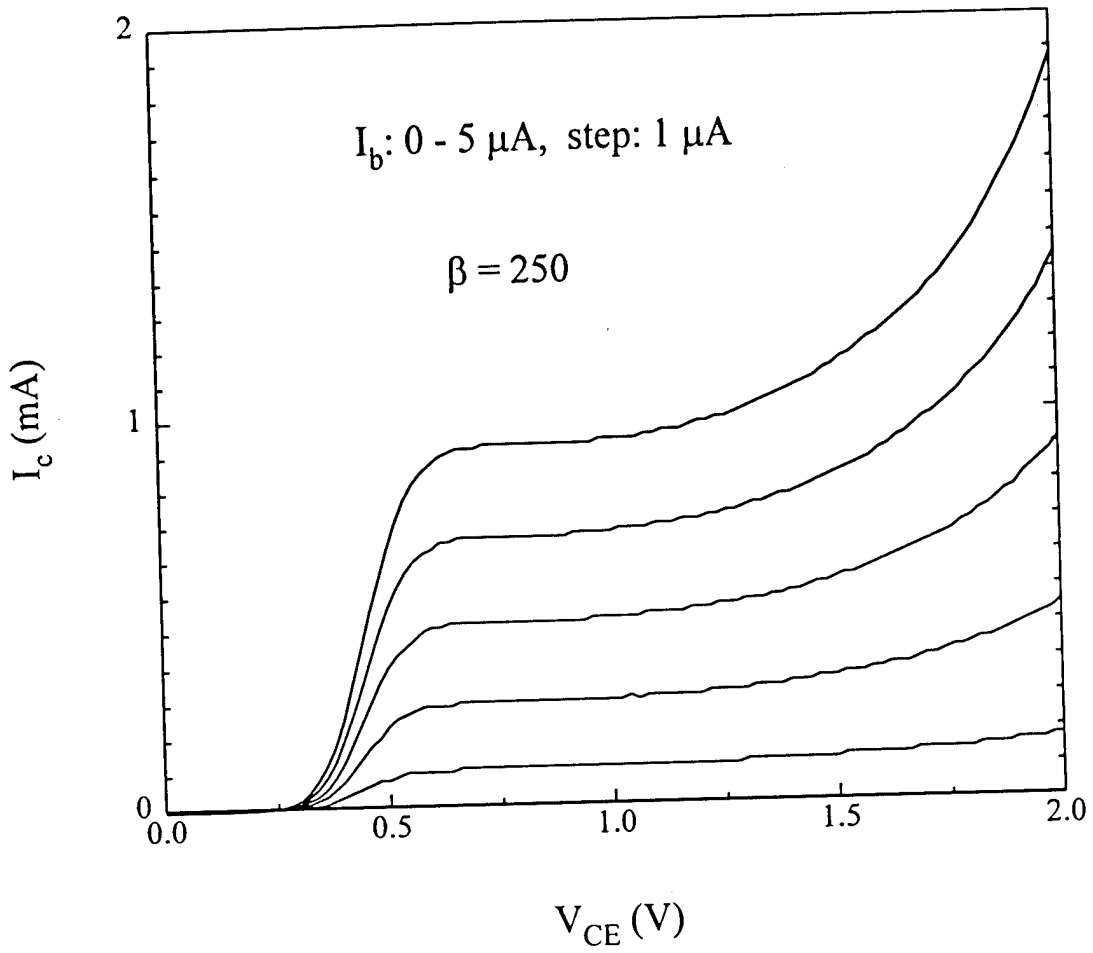

Fig. 4.3: The common emitter DC characteristic of an "average" HBT.

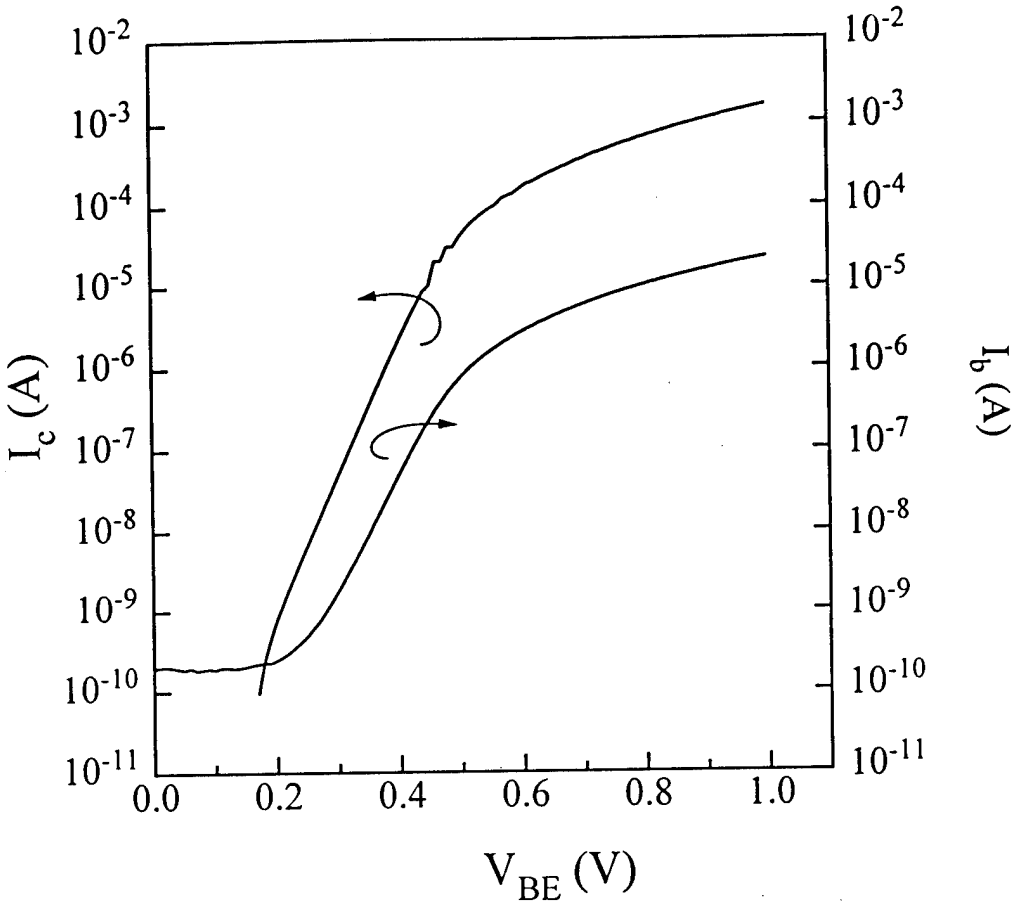

Fig. 4.4: The HBT Gummel plot.

4.2.3 FCSEL performance

The output device is a folded cavity surface emitting laser (FCSEL) which was surface bonded onto a pad adjacent to the pixel on the same wafer[22]. The light-current (L-I) curve for an average FCSEL is shown in Fig. 4.5. As seen in this plot, the threshold current (I_{TH}) was 24 mA, and the slope efficiency (η_d) was 17%. It was mentioned in Ch. 2 that the threshold current of the FCSEL determines the required pre-bias, which in turn determines the total pixel power dissipation. This limits the packing density, hence the need for lower threshold lasers. We also saw in Ch. 2 that the slope efficiency of the laser, η_d, affects the optical gain for the smart pixel. We have obtained I_{TH} = 20 mA and $\eta_d \leq 30\%$ for the best FCSEL devices.

4.2.4 Resistors

The value of the pixel feedback resistor was measured to be R_f=10 kΩ, instead of the designed value of 7 kΩ. The collector resistor, designed to be 2 kΩ, was measured to be 4 kΩ. The resistor values were largely affected by the alloyed n-type metal contact resistance. The p-metal contact also gave rise to high contact resistances. This high resistance was due to the non-alloyed p-contact, which was necessary to prevent punching the metal through the thin base. In the analysis in Ch. 2, we took the high p-type contact resistance into consideration for assigning the value of 1 kΩ to r_{bb}. Most of this resistance is due to the contact, as the sheet resistance of the base is only about 200 Ω. The Ti thin film resistors showed values within ±1 Ω of the target design.

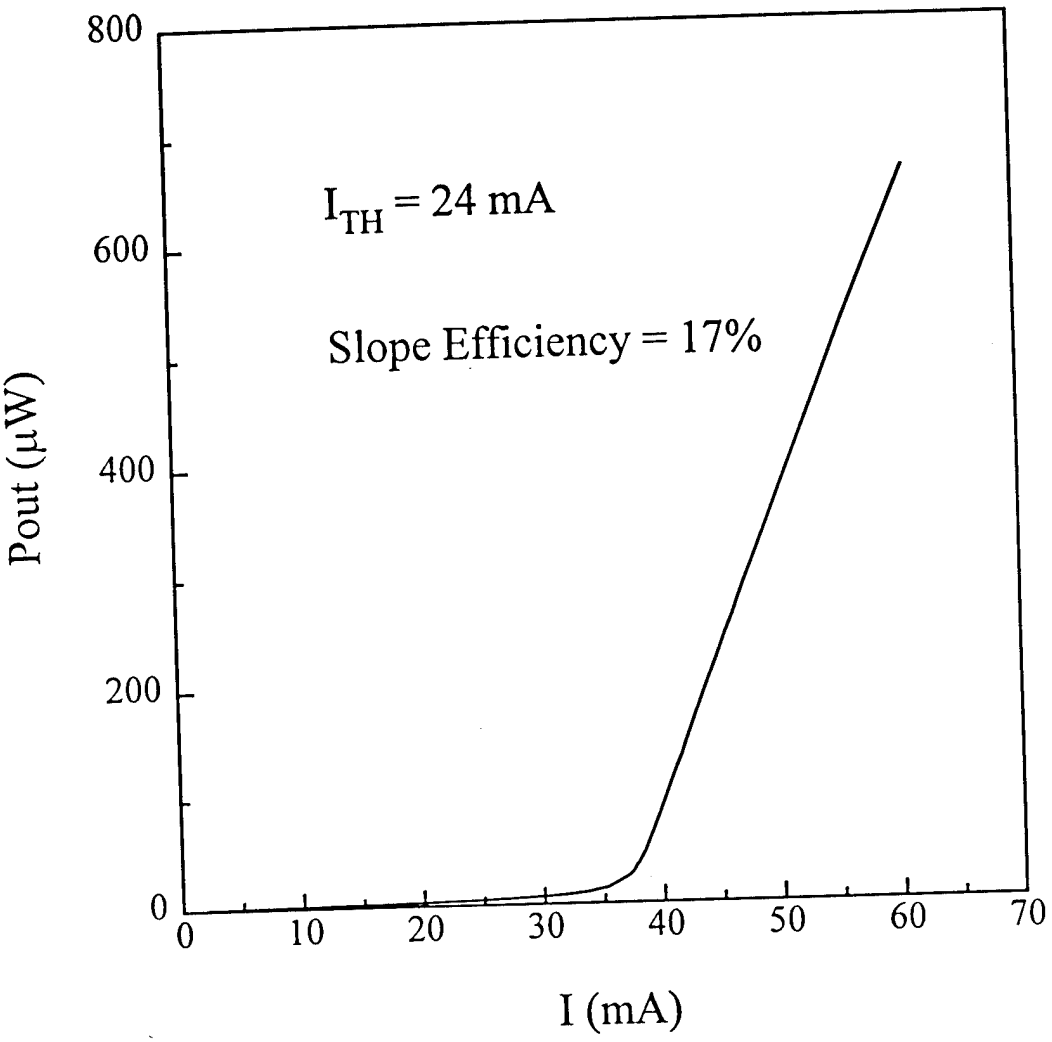

Fig. 4.5: The L-I curve for the FCSEL.

4.3 Smart Pixel performance

The smart pixel operates as follows: An optical input signal generates a negative voltage swing at the output of the front end. This, in turn, gives rise to a current swing in the differential pair, turning on the output FCSEL. Fig. 4.6 (a) shows the front end swing as a function of supply voltage for various levels of input optical power. It can be seen that the swing is almost the same for supply voltages of 2 and 3 V. Therefore, instead of using a bias supply of 3 V for all pixel components, we biased the front end and the input half of the differential pair at 2 V, and the output portion of the differential pair at 3 V. This reduced the total power dissipation of the circuit from 24 mW to 20 mW. In order to better comprehend the front end performance and compare it with the simulation results, Fig. 4.6 (b) shows the front end output swing as a function of the input optical power. The voltage swing was measured to be 0.3 V, and the input power level at the onset of saturation was about 50 μW. Thus, the front end performance is in good agreement with the simulation results obtained in Ch. 2.

The differential pair performance is presented in Fig. 4.7. This plot shows linear and uniform characteristics, indicating near identical performances for the paired HBT's. From this figure, we can calculate the transconductance of the pair, g_{md}, by measuring the change in the collector current of Q_3 as a function of the front end output swing (same as the base voltage of Q_2). For this voltage changing from 0.85 to 1.05 at a fixed value of base voltage of Q_2, ΔI_{c3}=0.7 mA, corresponding to g_{md}=7 mS. This is in good agreement with the simulated value of 5 mS.

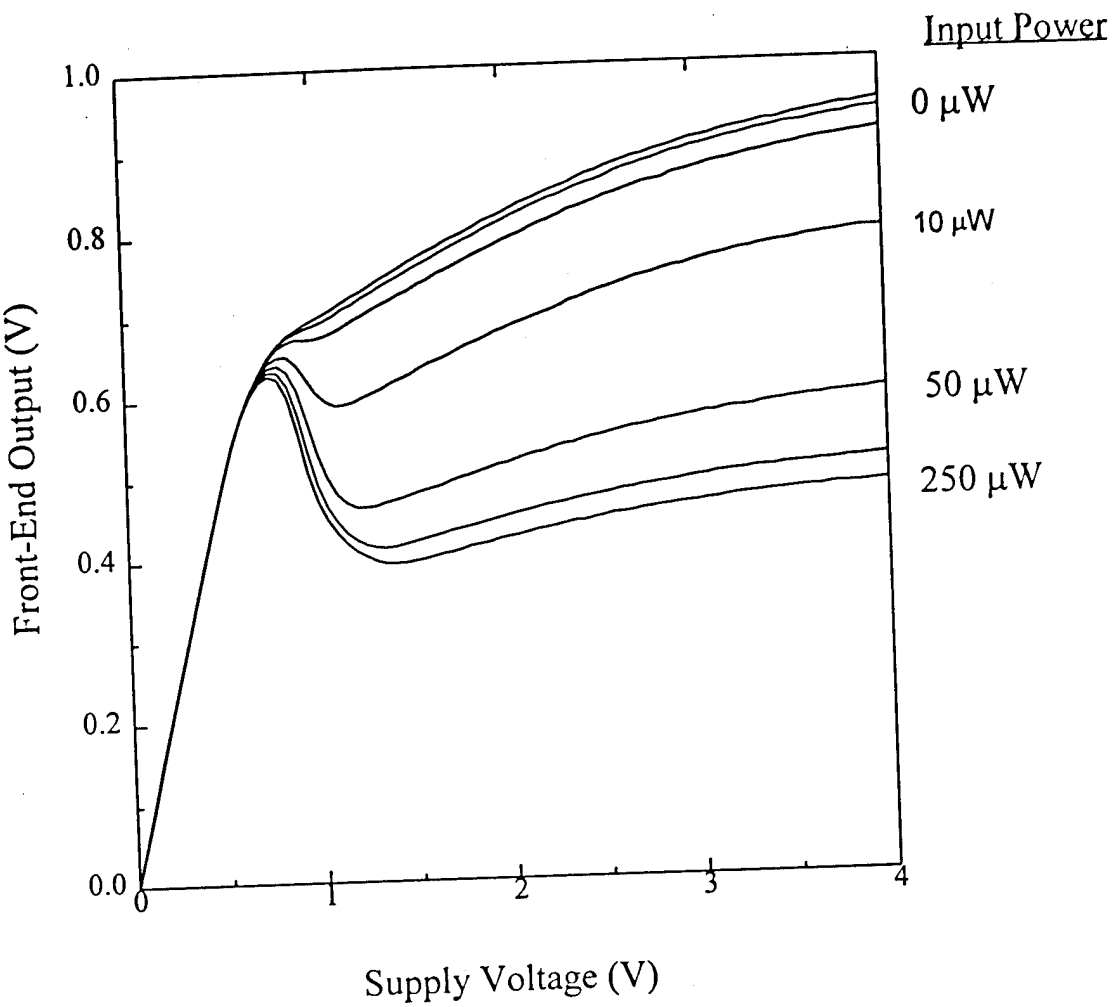

Fig. 4.6: The front end performance of the pixel (a) front end voltage swing as a function of the bias supply for different values of input optical power.

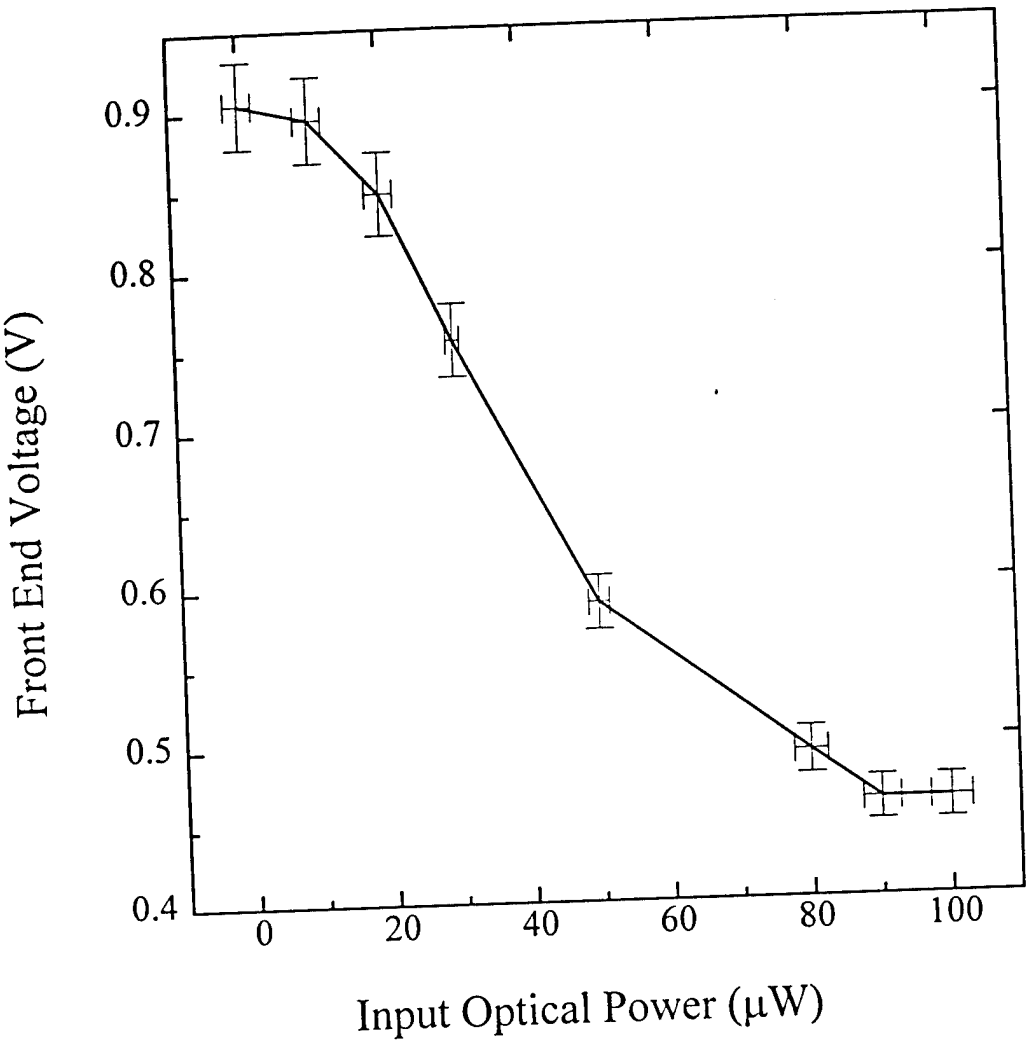

Fig. 4.6 (b): Front end voltage swing as a function of the input optical power.

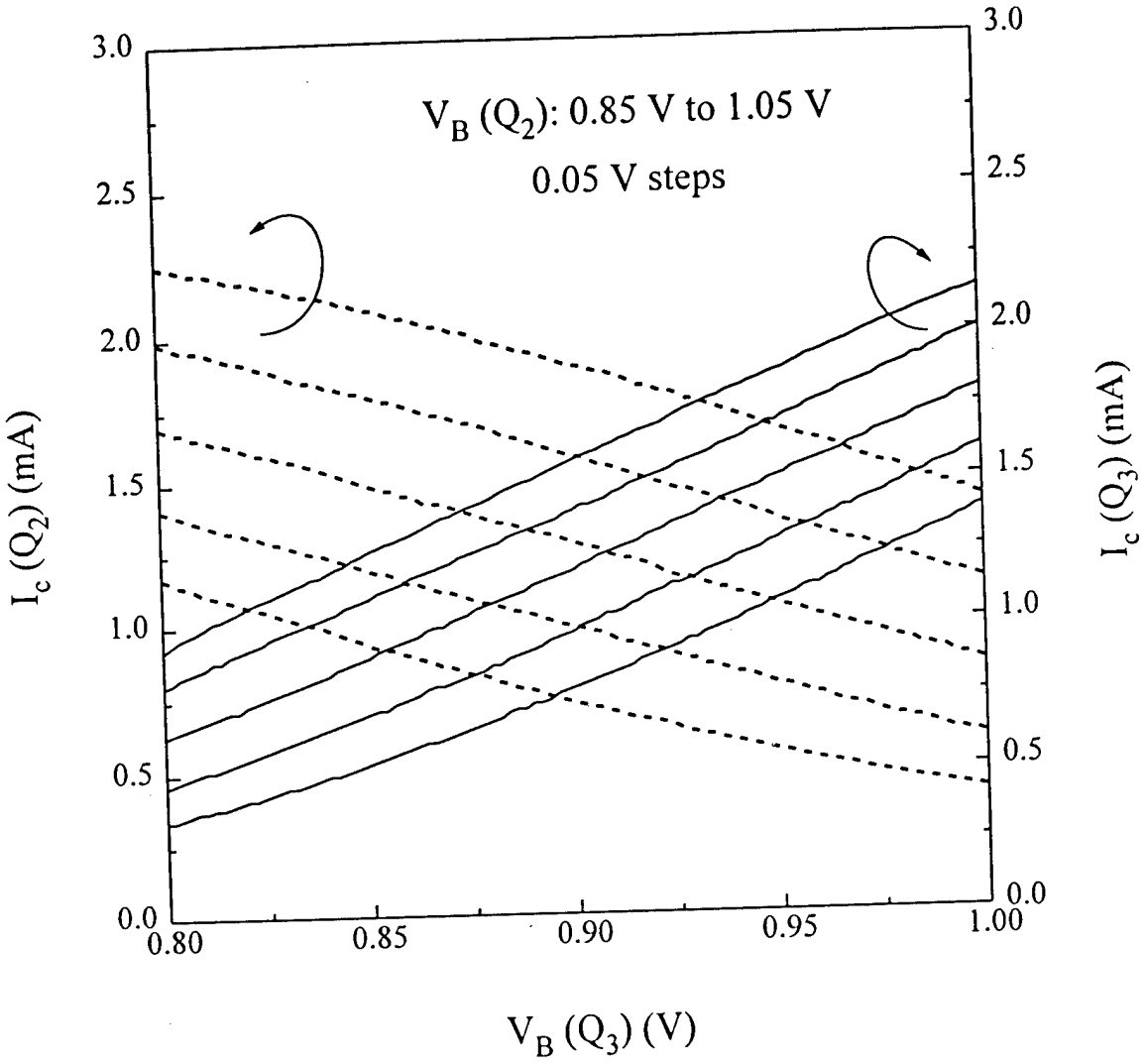

Fig. 4.7: The current swings of the differential pair as a function of base voltages.

The experimental set up used for optical characterization of the pixel is given in Fig. 4.8. In these measurements a 1.3 μm wavelength laser (ORTEL 3510A) was modulated by a sweep oscillator (HP 8350A) and used as the input optical source. The attenuator (HP 8156A) was used to control the input optical power level. The input was coupled into the pixel p-i-n photodetector using a single mode optical fiber. The quiescent bias to the pixel was supplied by an HP 4145 parameter analyzer. The surface mounted FCSEL was pre-biased at threshold by an external current source. The optical power emitted by the FCSEL was collected using a multimode fiber (to enhance coupling efficiency) and coupled into an Epitaxx InGaAs detector. The detector output was then measured using a picoammeter (Kiethley 617).

The optical I/O transfer function of the pixel and its derivative (defined as the optical differential gain, g_o) are presented in Fig. 4.9. Also shown is the large signal optical gain, G_o, defined as the ratio of output to input power. For input optical power, P_{in}, of up to 80 μW, we obtain $G_o = 2$ to 4, which is in agreement with the simulated result of 3. We also observe a maximum value of $g_o = 8$ for $P_{in} = 30$ μW. If we account for a 30% loss at the input due to the non-AR coated p-i-n detectors, the "internal" value of g_o is ~ 10. The output power levels off to 40 μW for P_{in} values up to about 25 μW, due to the laser being pre-biased just at threshold. This effect can be explained by returning to the laser L-I curve in Fig. 4.5. By choosing a certain pre-bias current, the laser operation efficiency is determined. At 24 mA, the laser efficiency is low, and requires a current swing large enough (P_{in}>25 mW) to enter the high efficiency region of operation. This pre-bias at the low efficiency regime (dictated by pixel total power-dissipation requirements) is also the cause for the drop in G_o and g_o at low power levels. For higher

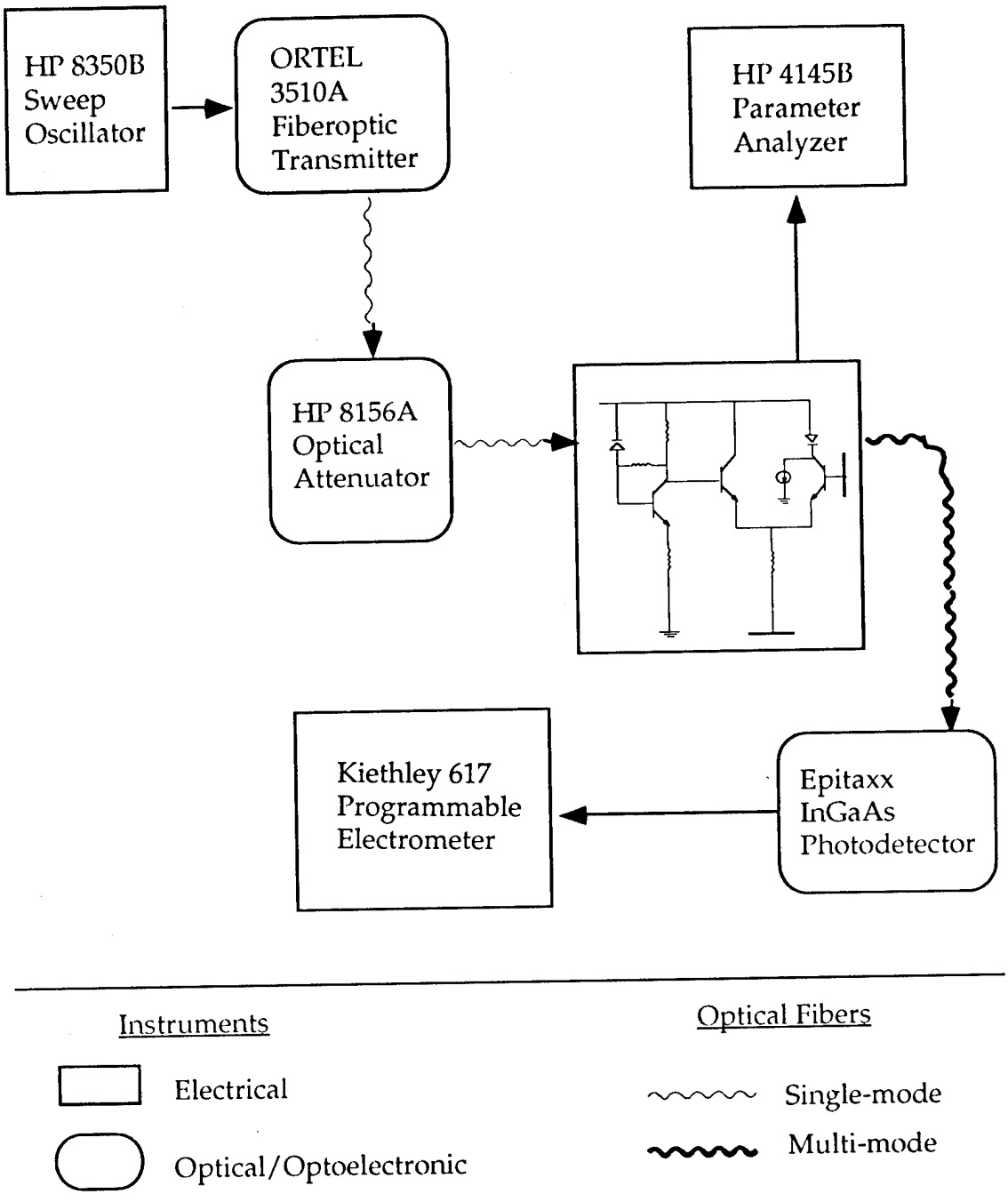

Fig. 4.8: The measurement set up for optical characterization of the smart pixel.

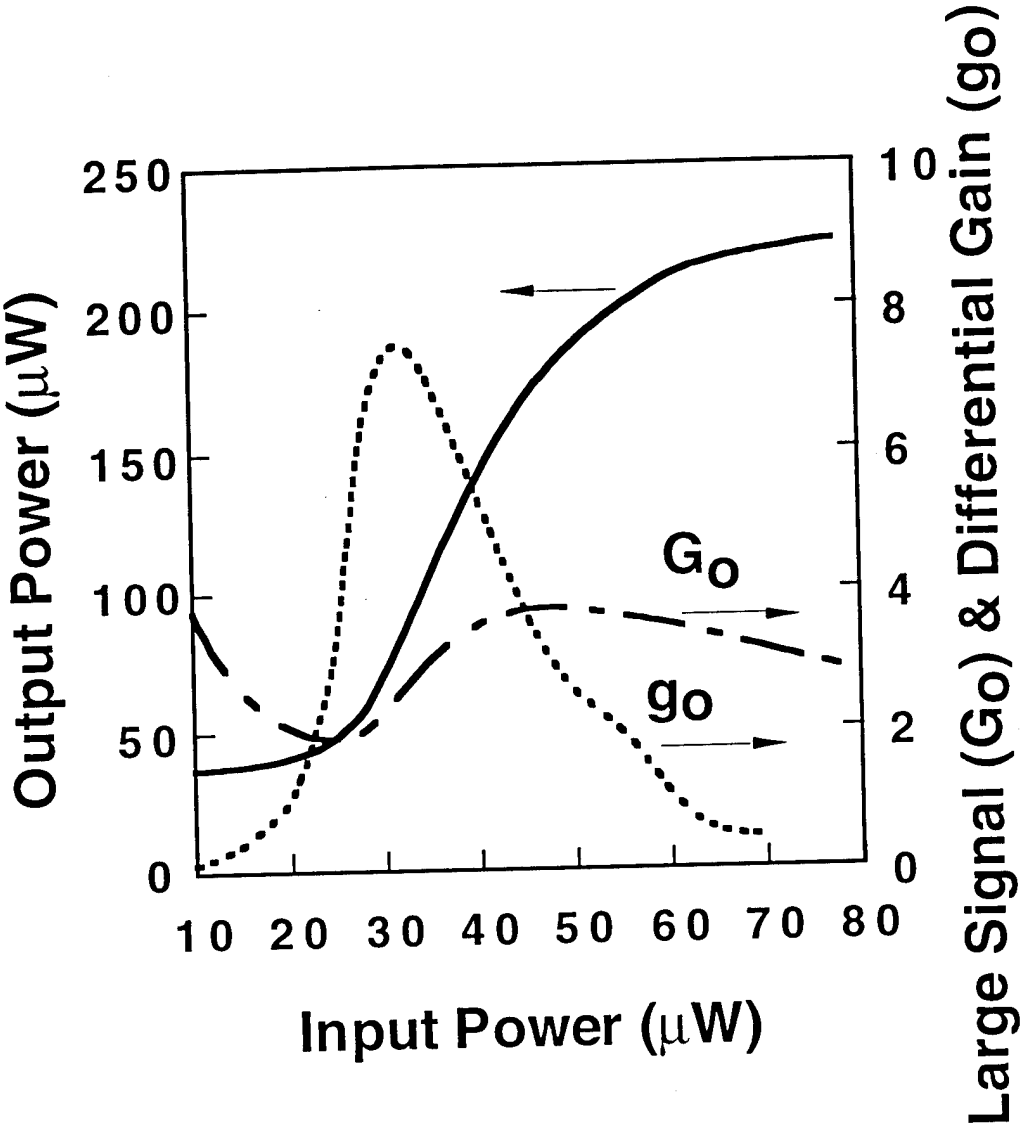

Fig. 4.9: The optical transfer function and the gain curves for the smart pixel.

power levels, the pixel is fully on and exhibits optical gain.

On the other hand, for P_{in} > 50-60 μW, Q_1 of the front end saturates, causing both g_o and G_o to decrease and the output to level off. In this regime, the pixel can be used as a thresholding circuit. However, as mentioned in Ch. 2, the speed degradation in the saturated regime of the front end, will limit the pixel functionality. From this plot, the maximum contrast ratio (CR) is ~5. All of the above curves were obtained assuming the following parameters: detector efficiency η_{ph}=65%, FCSEL slope efficiency, η_d=17%, and coupling efficiency η_c=30%.

The importance of cascadability for the functionality of an interconnect system was discussed in Ch. 2. Here, we study this criterion for the smart pixel. In Fig. 4.10, the ratio (R) of the output on/off power (C_o) to that of the input (C_i) is plotted as a function of C_i for different off-state input powers, $P_{in(off)}$. Optical cascadability, i.e. R≥1, can be achieved for off-state input powers ranging from 12 μW to 28 μW. As can be seen in Fig. 4.10, for an off-state input power of 12 μW, a maximum value of C_i = 6 while maintaining R≥1 is achieved. The on-state optical input power at this point is the product of C_i and the off-state input power, equal to 72 μW. From Fig. 4.9, this input power corresponds to G_o = 3. Cascadability cannot be achieved for off-state P_i < 12 μW. The drop in R for low C_i and P_{in} < 20 μW is related to the decrease in g_o in Fig. 4.9. The constraints on cascadability stem from the pre-bias output power and the pixel large-signal gain. Therefore, at low P_{in}, a trade-off exists between contrast ratio and gain vs. pixel sensitivity (i.e. the minimum required input power). The pixel is in its linear amplification

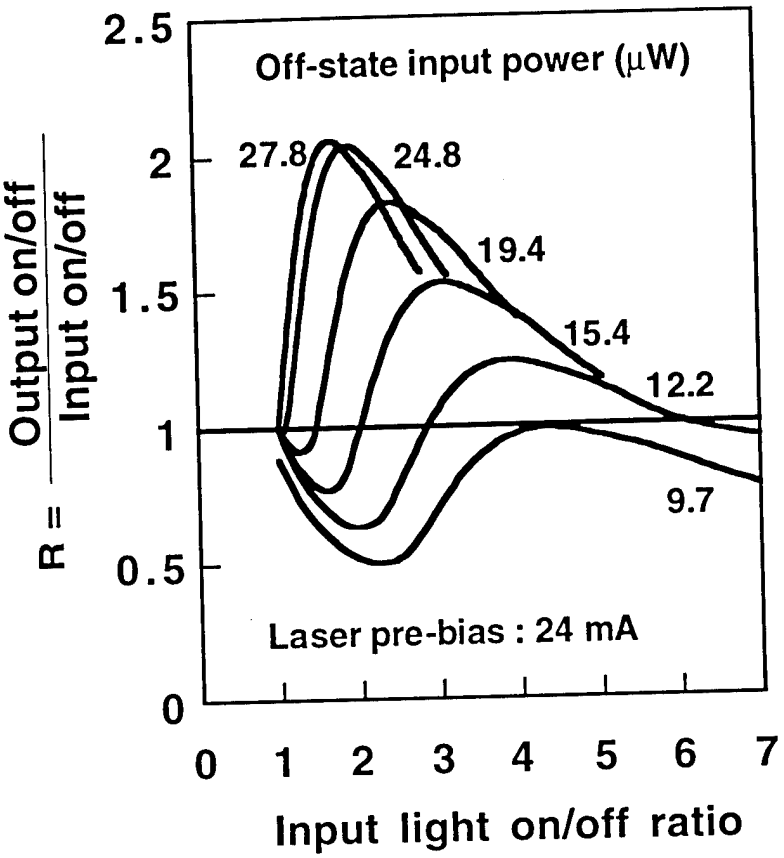

Fig. 4.10: Demonstration of cascadability for the smart pixel.

region for on-state input powers from 30 to 50 μW. Beyond this, the pixel gain saturates and hence, R decreases.

We have also measured the bandwidth and the sensitivity of the pixel with the same set shown in Fig. 4.8, but replacing the picoammeter by a spectrum analyzer (Tektronix 2753P). The frequency response of the pixel is given in Fig. 4.11. The 3-dB frequency was found to be about 50 MHz corresponding to 100 Mb/s assuming a non-return-to-zero, NRZ, coding scheme. We saw in Ch. 2 that the bandwidth is primarily limited by the base-collector junction capacitances (C_{bc}~300 fF), and the feedback resistor, R_f. As mentioned earlier, R_f=10 kΩ, making the expected bandwidth to be 53 MHz, which is very close to the measured value.

In order to calculate the pixel sensitivity, we use standard noise analysis for optical receivers[5]. The noise sources for a typical optical receiver fall into two general categories: Those which depend on the incident optical signal, and those which are independent of the signal level. The former involves the photogenerated current flowing in the detector in response to the incident optical signal, and the latter includes the contributions of the amplifier and the biasing circuit as well as the detector dark current. In order to obtain the minimum detectable power to achieve a desired signal-to-noise ratio, we focus on the latter category. The total mean square current referred to the amplifier input for a p-i-n/HBT receiver is the sum of the following terms: Shot noise ($\langle i_t^2 \rangle$) is due to all the quiescent currents that are present at the input of the circuit. Channel noise ($\langle i_{ch}^2 \rangle$) is due to the shot noise induced by the quiescent collector current referred to the input. Johnson (thermal) noise($\langle i_r^2 \rangle$) is due to the load (or feedback) resistor, and

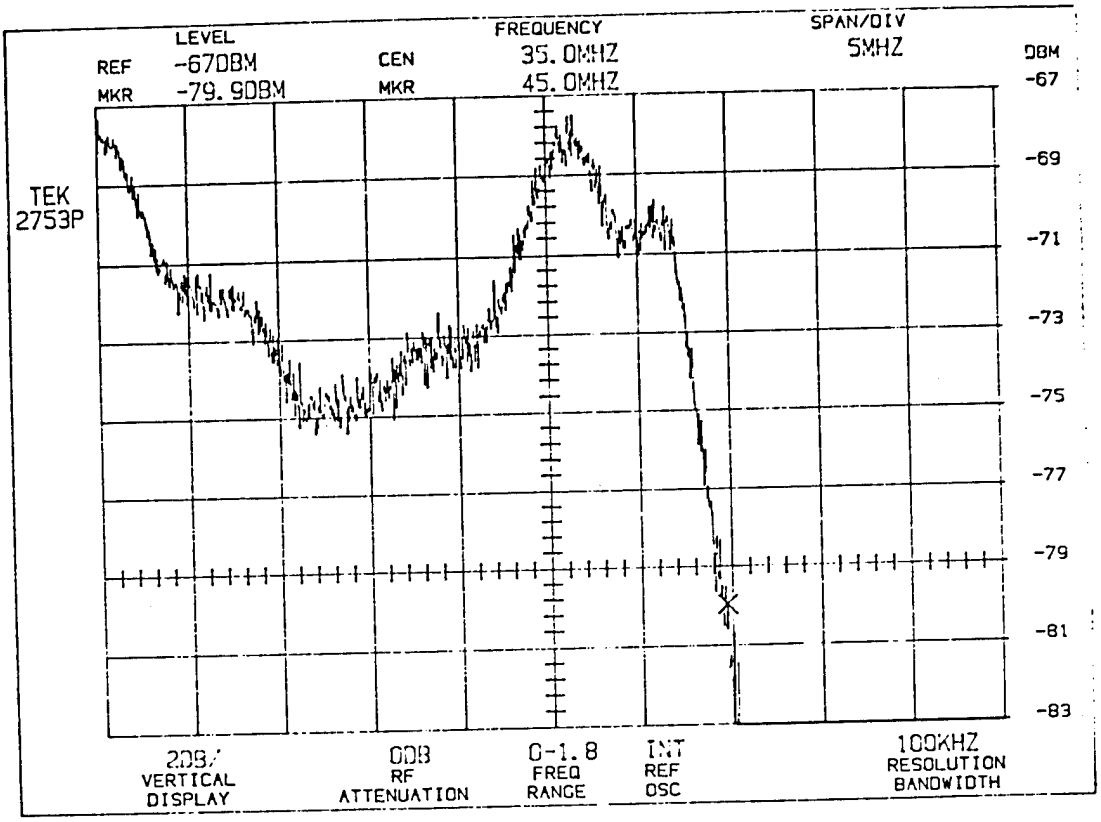

Fig. 4.11: The smart pixel bandwidth.

the base series resistance ($<i_{rb}^2>$). The expressions for these noise terms are as follows[6]:

$$<i_t^2> = 2qI_{DC}BI_2,$$

$$<i_{ch}^2> = \frac{2qI_c}{g_m^2}[(\frac{1}{R_f} + \frac{1}{r_{be}})^2 BI_2 + (2\pi C_T)^2 B^3 I_3],$$

$$<i_r^2> = \frac{4kT}{R_f} BI_2, \qquad (4.1).$$

$$<i_{rb}^2> = 4kTr_{bb}[\frac{BI_2}{R_f^2} + (2\pi)^2 (C_d + C_s)^2 B^3 I_3].$$

In this equation, q is the electron charge, k is Boltzmann's constant, T is the temperature, B is the data bit rate, I_{DC} is the quiescent current at the input, I_c is the quiescent collector current, g_m is the front end HBT transconductance, R_f is the feedback resistor, r_{be} is the dynamic base-emitter resistance, C_T is the total capacitance due to amplifier (C_a), detector (C_d) and stray capacitance associated with leads and package (C_s), r_{bb} is the base resistance, and I_2 and I_3 are the Personick integrals. These integrals depend on the transfer function of the circuit, and their values for a rectangular input and a raised cosine output pulse with an NRZ data format are approximately 0.5 and 0.1, respectively. It should be noted that in the smart pixel circuit, I_{DC} includes the quiescent base current as well as the detector dark current. Therefore, the noise currents can be re-written as:

$$< i_t^2 >= 2q(I_b + I_d))BI_2,$$

$$< i_{ch}^2 >= \frac{2qI_c}{g_m^2}[(\frac{1}{R_f} + \frac{1}{r_{be}})^2 BI_2 + (2\pi C_T)^2 B^3 I_3],$$

$$< i_r^2 >= \frac{4kT}{R_f} BI_2, \qquad (4.2).$$

$$< i_{rb}^2 >= 4kTr_{bb}[\frac{BI_2}{R_f^2} + (2\pi)^2 (C_d + C_s)^2 B^3 I_3].$$

It should be noted that the resistor R_e (Fig. 2.2) was bypassed in the pixel characterization, and hence its noise contribution is not included. Table 4.1 contains the list of device parameters used for this calculation. The total noise current for the p-i-n/HBT case, $<i_{pb}^2>$ can be written as:

$$< i_{pb}^2 >=< i_t^2 > + < i_{ch}^2 > + < i_r^2 > + < i_{rb}^2 > \qquad (4.3).$$

The sensitivity of a receiver is expressed in terms of the minimum time-averaged detectable power at a given bandwidth to ensure a desired bit error rate (BER), and is usually in units of dBm (0 dBm=1 mW). Hence, the sensitivity is given by[5]:

$$P_{min} = \frac{1+r}{1-r}\frac{Q}{\eta_{ph}}(\frac{hc}{q\lambda}) < i_{pb}^2 >^{1/2} \qquad (4.4)$$

where r is the extinction ratio defined as the ratio of power received in the off state, p_0, to that in the on state, p_1, or $r=p_0/p_1$, Q is the required signal-to-noise ratio to achieve a desired BER (Q=6 for BER=10^{-9}), h is Planck's constant, c is the speed of light in vacuum, λ is the operation wavelength,

Table 4.1

List of device parameters for the p-i-n/HBT receiver

Parameter	Definition	Value
I_b	base current	4 μA
I_d	detector dark current	20 nA
I_c	quiescent collector current	1 mA
g_m	transconductance $g_m=qI_c/kT$	0.04 A/V
R_f	feed back resistor	10 kΩ
r_π (r_{be})	base-emitter internal resistance $r_\pi = \beta/gm=\beta*kT/qI_c$	5.2 kΩ
C_T	total capacitance	1 pF
r_{bb}	base series resistance	1 kΩ
C_s	stray capacitance	0.5 pF
C_d	detector capacitance	0.1 pF

and η_{ph} is the external quantum efficiency of the detector. We measure for our pixel: η_{ph}=0.65, and r=0.65.

From the above expressions, a pixel sensitivity of $<P_{min}>$ = -33.5 dBm was calculated. The minimum average input optical power (assuming 50% duty cycle), $<P_{min}>$, needed to achieve SNR = 6 (8 dB) at 100 Mb/s, was measured for our pixel to be 700 nW. From this value, we infer a pixel sensitivity of -32 dBm for an NRZ coding scheme. This is within 1.5 dB of the calculated value. The discrepancy could be due to the noise in the output stage of the pixel which was ignored in this analysis. A SNR = 8 dB is maintained for input peak powers ranging from 1.4-80 μW, corresponding to a dynamic range of ~ 18 dB.

4.4 Switching energy considerations

The mean switching energy of the pixel is a function of the minimum required power and the bandwidth, Δf, as follows:

$$< E_{sw} > = < P_{min} > /\Delta f \qquad (4.5).$$

At 100 Mb/s, we measure $< E_{sw} >$ = 14 fJ. Since under these conditions, G_o ~ 1, and R<1, the pixel cannot drive subsequent stages while maintaining the same SNR and hence is not cascadable. On the other hand, when operated at R≥1, the pixel can switch with a small input power swing of 3 μW (27.7 μW to 30.7 μW) at 100 Mb/s, which corresponds to a 30 fJ switching energy. To the best of our knowledge, this is the lowest switching energy reported to date for a cascadable smart optical transceiver. Under these conditions, G_o = 3 and R>1, which allow for fan-out and compensation for coupling loss in a cascaded, multi-stage system.

Among various approaches to smart pixels are FET-SEED's[7], VCSEL-based technologies[8,9], and InP-HBT/phototransistor (HPT) pixels[10]. Although optical gain and cascadability have been demonstrated with both FET-SEED's and VCSEL-based pixels, these technologies have only been implemented at 0.85 μm wavelength, hence rendering them incompatible with long-haul fiber optics applications. Previously demonstrated InP-HBT/HPT-based pixels could not be used for vertical I/O geometries, as they employed external edge-emitting lasers for their output device. While maintaining cascadability (R≥1), the measured minimum switching energy of 30 fJ at 100 Mb/s for our pixel is 200 times lower than VCSEL-based transceivers[8,9], and three times lower than for FET-SEED's[7]. In comparison with previously reported InP-HBT/HPT based smart pixels, our pixel has 100 times lower E_{sw}, and 3 times greater differential gain[10]. This low switching energy is mainly due to the significant HBT gain down to low current levels, and the feedback.

Sensitivities and switching energies are shown to be comparable for conventional optical receivers using either a hybrid[11], or a monolithic OEIC approach[12], where $< E_{sw} > \sim 1$ fJ. As a simple receiver, our pixel sensitivity of -32 dBm at 100 Mb/s is within 8 dB of the best reported values for hybrid and OEIC receiver technologies, however, it demonstrates considerably lower power dissipation. The results for various smart pixel technologies are summarized in Table 4.2.

Table 4.2

Switching energy considerations

for smart pixel technologies

Approach	Sensitivity @100 Mb/s	Switching Energy	Photons/bit	Max. Bandwidth	Ref.
Hybrid	-40 dBm	1 fJ	$5x10^3$	10 Gb/s	11
OEIC recv'r	-40 dBm	1 fJ	$5x10^3$	2.4 Gb/s	12
FET SEED	---	100 fJ	$5x10^5$	2 Gb/s	7
VCSEL pixel	---	6 pJ	$3x10^7$	200 Mb/s	8,9
InP pixel	-18 dBm	3.8 pJ	$1.9x10^7$	80 Mb/s	10
FCSEL pixel	-32 dBm	30 fJ	$1.5x10^5$	100 Mb/s	*

*: This work.

4.5 Temperature dependence of pixel components

4.5.1 P-i-n temperature dependence

The expressions that govern noise in the smart pixel, given in Eq. 4.2, are mostly temperature dependent, where the pixel sensitivity can be improved by reducing the operation temperature. It is important to know how different pixel elements will function in lower temperature regimes. The dark current is a result of generation-recombination(g-r), and surface recombination: $I_d = I_{g\text{-}r} + I_{surface}$. The expression for generation-recombination current is[13]:

$$I_{g-r} = \frac{qn_iAW}{\tau_{eff}}[exp(\frac{qV}{2kT}) - 1] \tag{4.6}$$

where n_i is the intrinsic carrier concentration, A is device area, W is the depletion region width, τ_{eff} is the effective carrier lifetime, and V is the applied junction voltage, which is negative for reverse bias. The intrinsic carrier concentration is defined as:

$$n_i = \sqrt{N_c N_v}\, exp(-\frac{E_g}{2kT}) \tag{4.7}$$

where E_g is the band gap, and N_c and N_v are the effective density of states for conduction and valence bands. They are defined as:

$$N_c = 2(\frac{2\pi m_n^* kT}{h^2})^{3/2} \quad , \quad N_v = 2(\frac{2\pi m_p^* kT}{h^2})^{3/2} \tag{4.8}$$

where m^*_n and m^*_p are the effective electron and hole mass. Hence, the temperature dependence of n_i is of the form:

$$n_i \sim T^{3/2} exp(-\frac{E_g}{2kT}) \qquad (4.9).$$

Since V<0, exp(qV/2kT)~0, and hence the temperature dependence of the $I_{g\text{-}r}$ can be written as:

$$I_{g-r} \sim - \frac{T^{3/2}}{\tau_{eff}} exp(-\frac{E_g}{2kT}) \qquad (4.10).$$

The surface recombination current is defined as:

$$I_{surface} = 2qn_i \pi dWS \qquad (4.11)$$

where $2\pi dW$ is the surface area of the junction, and S is the surface recombination velocity, defined as:

$$S=\sigma_s v_{th} N_{st} \qquad (4.12)$$

where σ_s is the carrier capture cross section, v_{th} is the carrier thermal velocity, and N_{st} is the density of surface traps. The expression for the thermal velocity is:

$$v_{th} = \sqrt{\frac{3kT}{m^*}} \qquad (4.13).$$

Hence, the temperature dependence of the surface recombination current, assuming that N_{st} is constant and including the temperature dependence of n_i, will be:

$$I_{surface} \sim T^2 exp(-\frac{E_g}{2kT}) \qquad (4.14).$$

Thus, the temperature dependence of both of $I_{g\text{-}r}$ and $I_{surface}$ mechanisms is dominated by the exponential terms. The dark current of the p-i-n as a

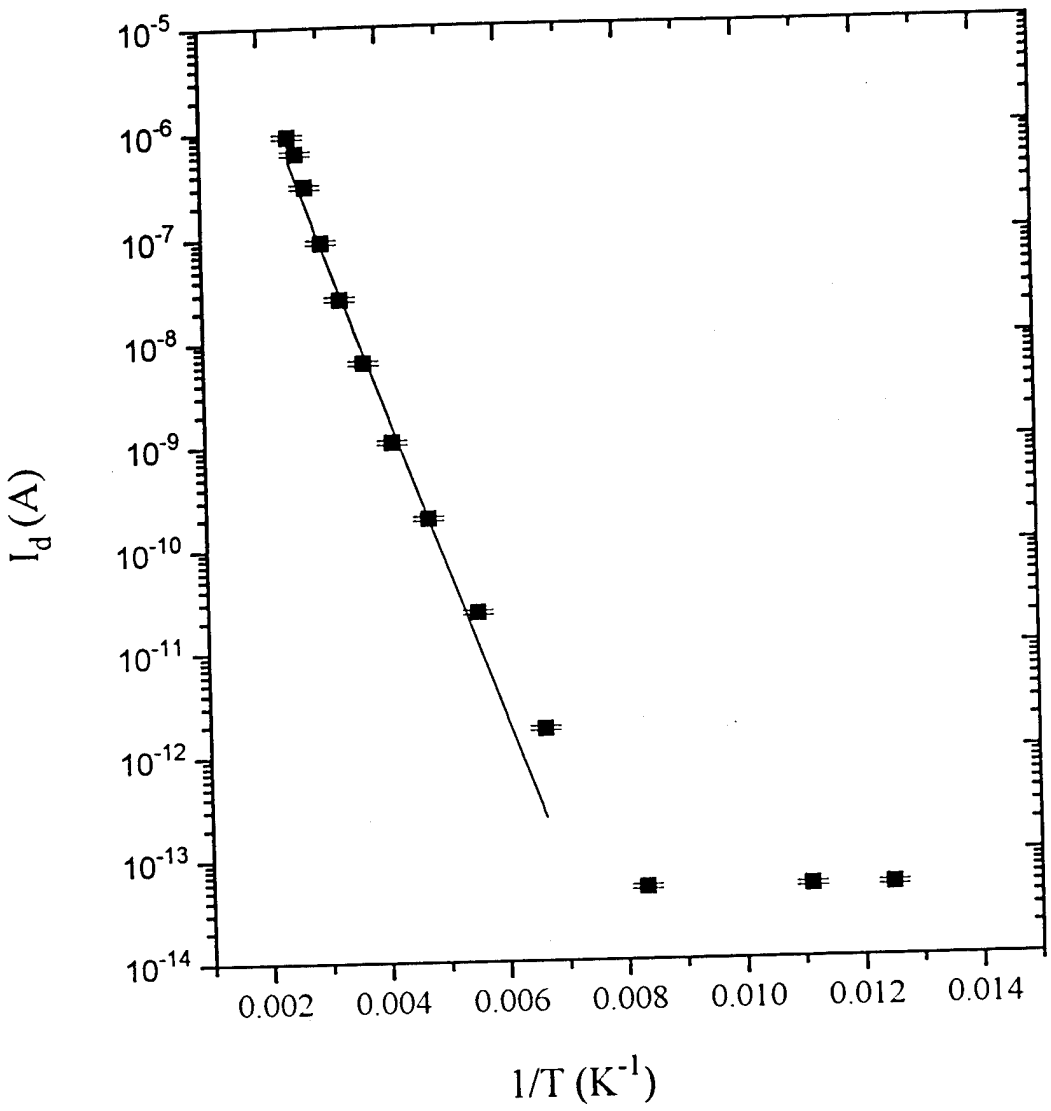

Fig. 4.12: The variation of p-i-n dark current with temperature. The lowest limit of the measured current was set at 10^{-13} A by the instrument.

function of temperature is plotted in Fig. 4.12. The data show a good fit to these expressions, with an effective activation energy of 0.3 eV.

The absorption constant, and hence, the p-i-n detector efficiency have a weak dependence on temperature as a result of the change in band-gap. However, the wavelength spectrum of the detector sensitivity is broad-band to the extent that its efficiency is not expected to change considerably.

4.5.2 HBT temperature dependence

The HBT's used in the smart pixel also have temperature dependent behavior. Several researchers including ourselves have found that the HBT current gain β, base-emitter voltage V_{be}, reverse saturation current I_{SE}, and ideality factors are functions of temperature[14-16]. In our measurements, V_{be}, β, and the ideality factor increases, while I_{SE} decreases as the temperature is lowered.

The base-emitter junction is forward biased, and hence V_{be} is nearly identical to the built-in potential for that junction. The expression for the built-in potential for an abrupt non-degenerate N-p^+ heterojunction is[17]:

$$V_{bi} = \{E_{g1}+[\Delta E_c-(E_{c2}-E_{f2})]-(E_{f1}-E_{v1})\}/q \qquad (4.15)$$

where E_{g1} in this case is the band gap of InGaAs equal to 0.76 eV, ΔE_c is the conduction band discontinuity which for InGaAs/InP heterojunctions is 0.24 eV, E_{c2}-E_{f2} is the energy difference between the conduction band and the Fermi level in the emitter, and E_{f1}-E_{v1} is the energy difference between the valence band edge and the Fermi level in the base. In Eq. 4.15 we can make the following approximation:

$$E_{c2}-E_{f2} = -kT\ ln(n/N_c) \qquad \text{and} \qquad E_{f1}-E_{v1} = -kT\ ln(p/N_v) \tag{4.16}$$

where n and p are the doping levels in the emitter and base, respectively. For $n<N_c$ and $p<N_v$, we have $\ln(n/N_c)<0$ and $\ln(p/N_v)<0$. Hence,

$$V_{bi} = \{E_{g1}+[\Delta E_c-kT\ln(N_c/n)] - kT\ln(N_v/p)\}/q \tag{4.17}$$

therefore,

$$\frac{\nabla V_{bi}}{\nabla T} = -\frac{k}{q}[\ ln(\frac{N_c}{n}) + \ ln(\frac{N_v}{p}) \ + 3] \tag{4.18}$$

where the temperature dependence of N_c and N_v is that of Eq. 4.8. The above expression predicts a negative and linear temperature gradient for V_{bi} with expected slope of -5×10^{-4} V/K. Further, for temperatures near zero, V_{bi} should approach $E_{g1}+\Delta E_c$=1.0 eV. Fig. 4.13 shows the change in V_{be} as a function of temperature for a fixed collector current of 1 mA, with the measured slope= -1.45×10^{-3} V/K. The base and emitter of our HBT's are both degenerate. That implies that Eq. 4.15 is an approximation, as in the degenerate case the true dependence of carrier density on the position of the Fermi level with respect to the band edge is sub-exponential. It therefore follows that the measured slope would be higher than the prediction. The intercept, however, does not depend on the degeneracy, and matches the theoretical prediction well

The base and collector ideality factors increase for lower temperatures: n_c changes from 1.1 to 1.3 , and n_b changes from 1.6 to 1.7. The temperature dependence in ideality factors has been observed before for similar structures[14]. This effect has been speculated to be related to the change in I_{SE}, which in turn is related to the V_{be} change as a function of temperature[18,19].

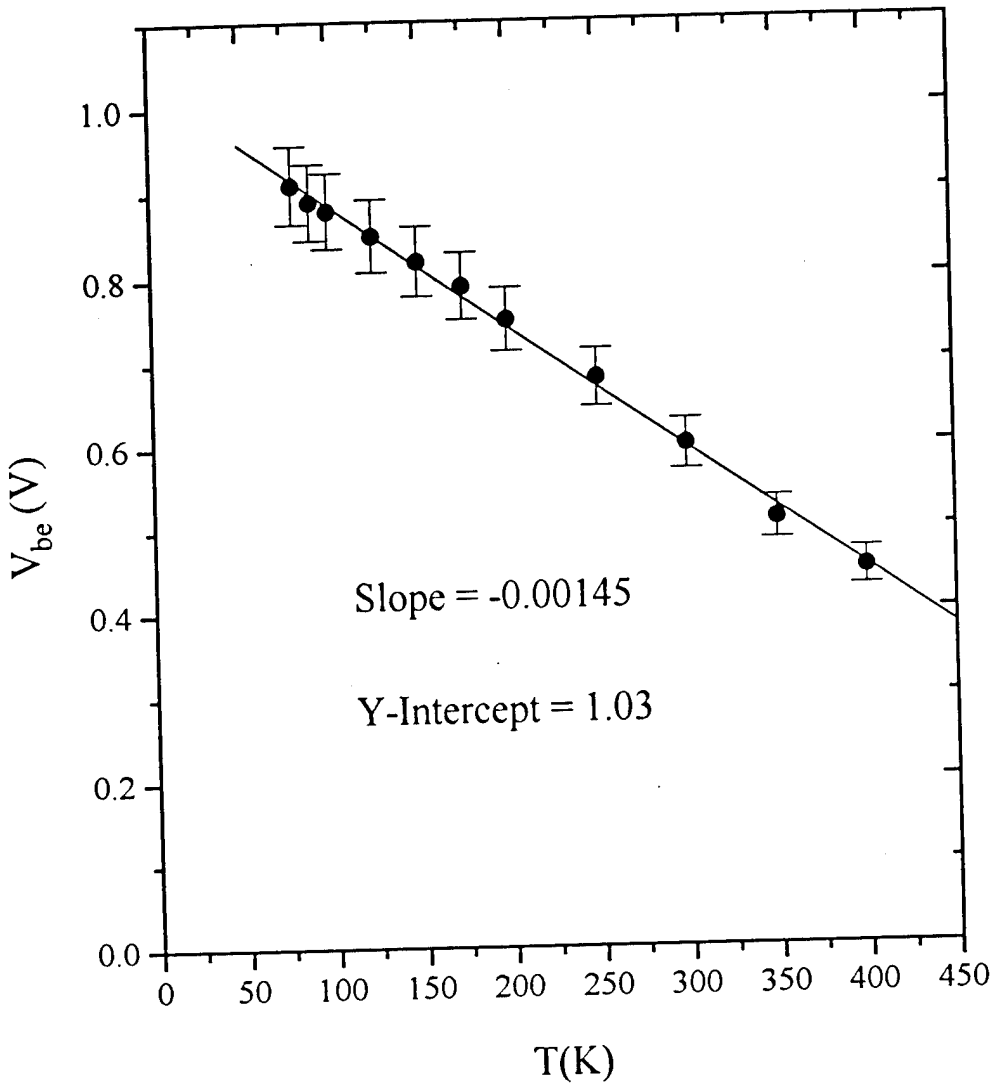

Fig. 4.13: Temperature dependence of V_{be} for collector current I_c=1mA.

The saturation current, I_{SE}, is defined as:

$$I_{SE} = \frac{qADn_i^2}{N_A W_B} = \frac{qA}{N_A W_B}\frac{kT}{q}\mu N_c N_v \exp(-\frac{E_g}{kT}) \qquad (4.19).$$

In the above expression, q is the electron charge, A is the base-emitter junction area, D is the diffusion constant of electrons in the base ($D=kT\mu/q$), N_A is the acceptor density in the base, and W_B is the base width. It has been demonstrated that the temperature dependence of mobility in InP down to about 80K can be expressed as[20]: $\mu \sim T^{-2}$. Hence, the temperature dependence of I_{SE} can then be written as:

$$I_{SE} \sim T^2 \exp(-\frac{E_g}{kT}) \qquad (4.20)$$

therefore, it is expected that I_{SE} would decrease with low temperature. Fig. 4.14 shows the behavior of I_{SE}/T^2 with temperature. The value for E_g deduced from the data is 0.65 eV.

The behavior of β as a function of temperature is shown is Fig. 4.15. It can be seen that β increases at lower temperature and then saturates. This behavior has been observed by other groups[15,21], and has been explained using the following expression for β:

$$\beta = \frac{\gamma\alpha}{1 - \gamma\alpha} \qquad (4.21).$$

where γ is the emitter injection efficiency, and α is the base transport factor. From this relation, it is obvious that unless γ is comparable to α, the value of β is determined by the smaller of γ and α. Although the exact nature of the dependence of β on temperature is uncertain, it appears from the data that the temperature dependencies of the reverse hole current (limiting γ) and

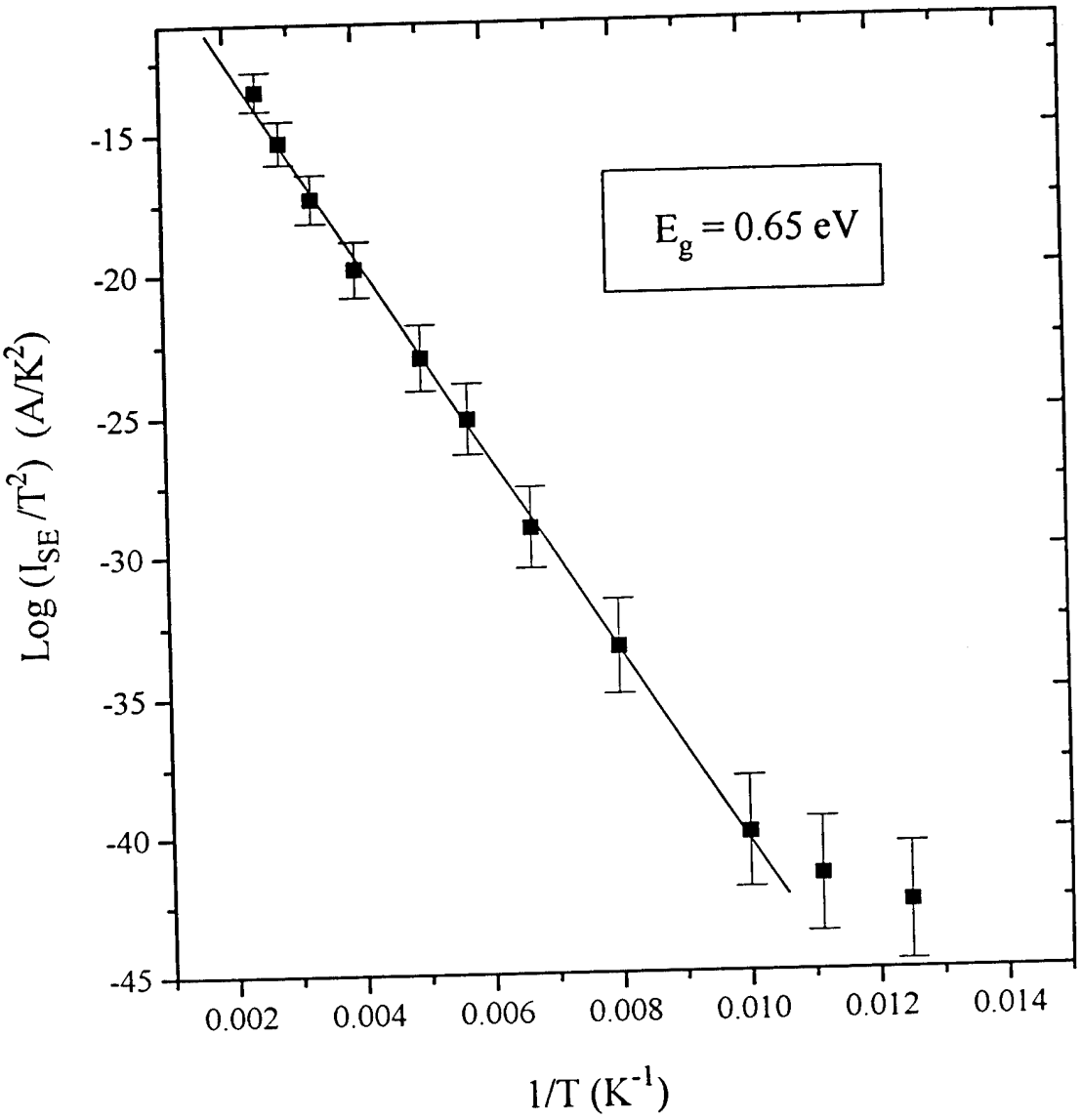

Fig. 4.14: The temperature dependence of HBT reverse saturation current, I_{SE}.

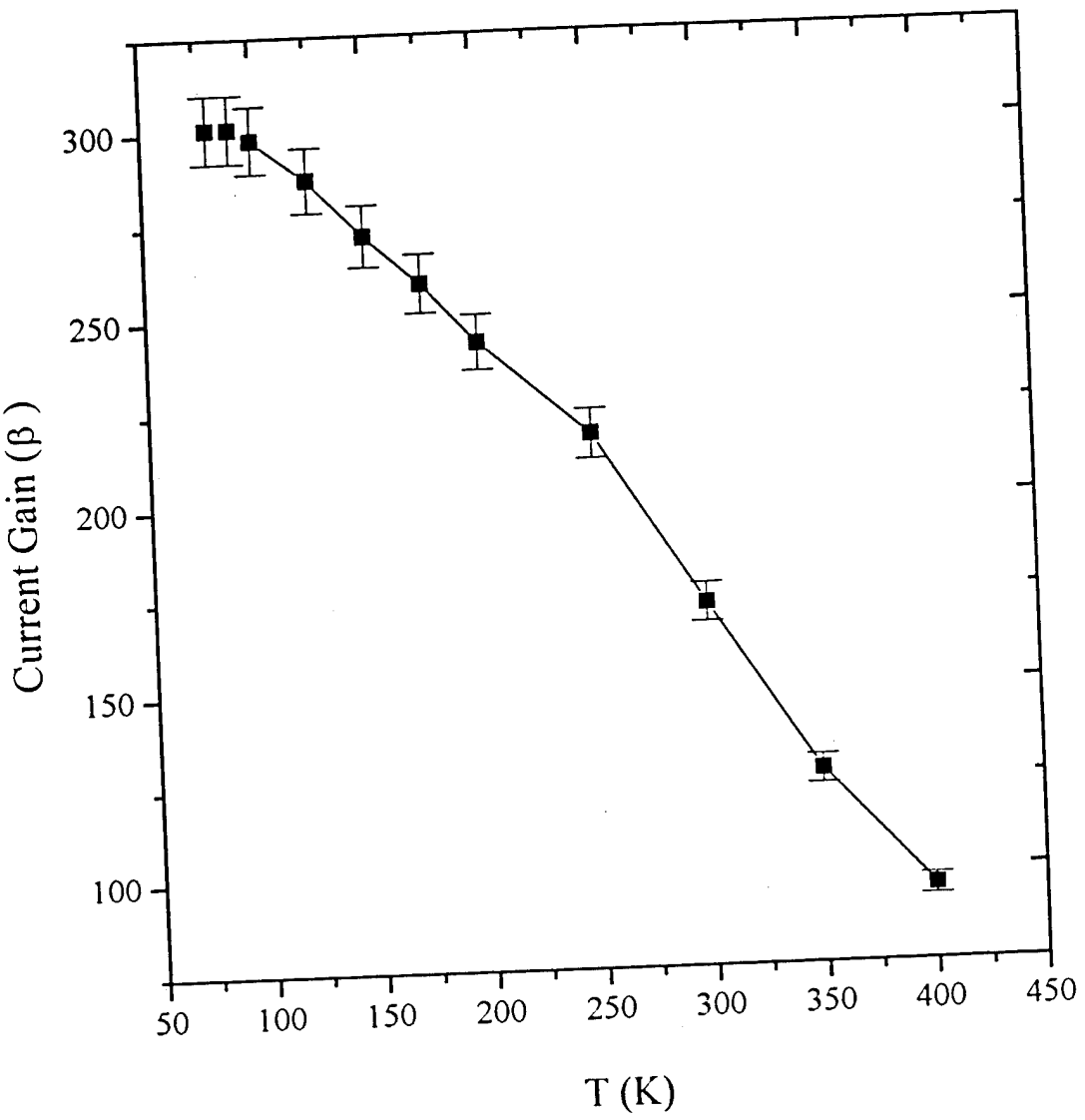

Fig. 4.15: The variation of the HBT current gain, β with temperature.

the recombination current (limiting α) cancel out at low temperature[15]. Hence, β saturates in this regime.

For InP/InGaAs HBTs, β has been shown both to increase[15], and to decrease[14] with temperature. This difference has been attributed to the nature of the base-emitter junction. For abrupt junctions, β increases and then saturates at low temperatures. On the other hand, in compositionally graded HBT's, β increases and then decreases towards zero at low temperatures. Although there is not yet a clear explanation of this effect, Enquist et al.[21] seem to clarify this discrepancy. They refer to the difference in electron transport between graded versus abrupt junctions as the mechanism causing the difference in temperature behavior. The spike barrier in the conduction band in abrupt junctions causes electron injection into the base above the band edge. These carriers gain higher energy for their non-equilibrium transport across the base. On the other hand, for graded junctions, the electrons are injected at the band edge with the same temperature as the lattice. This implies that the transport in graded junctions takes place under thermal equilibrium, but in abrupt junctions, non-equilibrium transport is dominant. The difference in the energy of the carriers compared to the lattice in these two cases is considered to be responsible for different dependencies of β on temperature. According to this theory, our data confirms the abruptness of the base-emitter junction. It should be mentioned that β shows a different temperature dependent behavior for different materials. In AlGaAs/GaAs, the dependence of β on temperature is similar to the InP material system[21]. In Si, β decreases at lower temperatures[22]. This observation was explained by the band gap shrinkage in the heavily doped emitter.

4.5.3 Temperature dependence of FCSEL

In Fig. 4.16 we show the threshold current of the FCSEL laser as a function of temperature[23]. The straight lines assume that the temperature dependence of the threshold current follow the empirical expression[24]:

$$I_{TH} = I_{TH0} exp(\frac{T}{T_0}) \tag{4.22}$$

where I_{TH0} is the temperature independent threshold current, T_0 is the characteristic temperature, and T is the measurement temperature. We have obtained T_0 values of 43K, 84K and 224K for the FCSEL as the measurement temperature is lowered. A lower value of T_0 implies that the threshold current increases more rapidly with increasing temperature. The change in T_0 for different temperatures indicates that the importance of each mechanism which determine I_{TH} varies with temperature. This behavior has been observed repeatedly for FCSEL's as well as for VCSEL's[25].

Furthermore, the slope efficiency is also a weak function of temperature, and is improved with cooling[22,26]. The lowering of threshold current with decreasing temperature can be advantageous. The laser pre-bias and hence the DC power dissipation can be lowered with decreasing temperature. Similarly, the improved slope efficiency at low temperature will result in a better optical gain, and increased fan-out.

4.5.4 Semiconductor Resistors

We saw in previous sections that the feedback resistor, R_f, had an important role in determining both the gain and the bandwidth of the smart pixel. The temperature dependence of R_f has been shown in Fig. 4.17. If the measured value for R_f was dominated by bulk resistivity, one would expect a

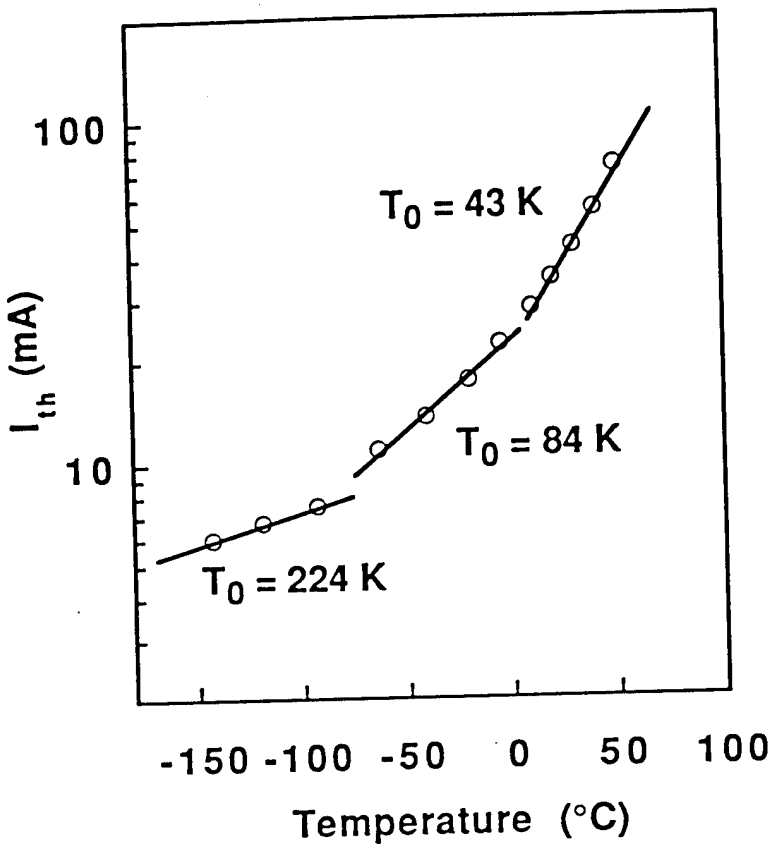

Fig. 4.16: The variation of the FCSEL threshold current with temperature.

decreasing behavior at lower temperatures due to the increase of mobility (μ) via:

$$R_f = \rho \frac{l}{A} = \frac{L}{q\mu nA} \tag{4.23}$$

where ρ is the material resistivity, l is the length of the resistor, a is the cross sectional area, μ is the electron mobility and n is the carrier concentration. The increasing behavior of R_f indicates that contact resistance is dominating, which can be expressed as[27]:

$$R_{con} = \frac{kT}{qAA^*} e^{\Phi/kT} \tag{4.24}$$

where A is teh contact area, A^* is teh Richardon's constant, and Φ is teh barrier heigth. In the inset of Fig. 4.17, $\mathrm{Ln}(R_{con}/T)$ is plotted vs. 1/T, indictaing a good fit to Eq. 4.24. The measured value of the feedback resistor increases by a factor of 7 as the temperature is lowered from 300 down to 77K.

4.6 Section Summary

Let us now speculate how temperature dependence of individual device characteristics effect the overall pixel performance. At lower temperatures, the pixel gain is expected to improve, as it is proportional to $g_m(=qI_c/kT)$, R_f and the laser slope efficiency. The improved slope efficiency of the laser will result in better optical gain. Due to the change in circuit characteristics, we can estimate the optical gain to increase by about 27 times at 77K compared to room temperature. However, the larger value of R_f implies that the maximum detectable power is going to be much smaller, as

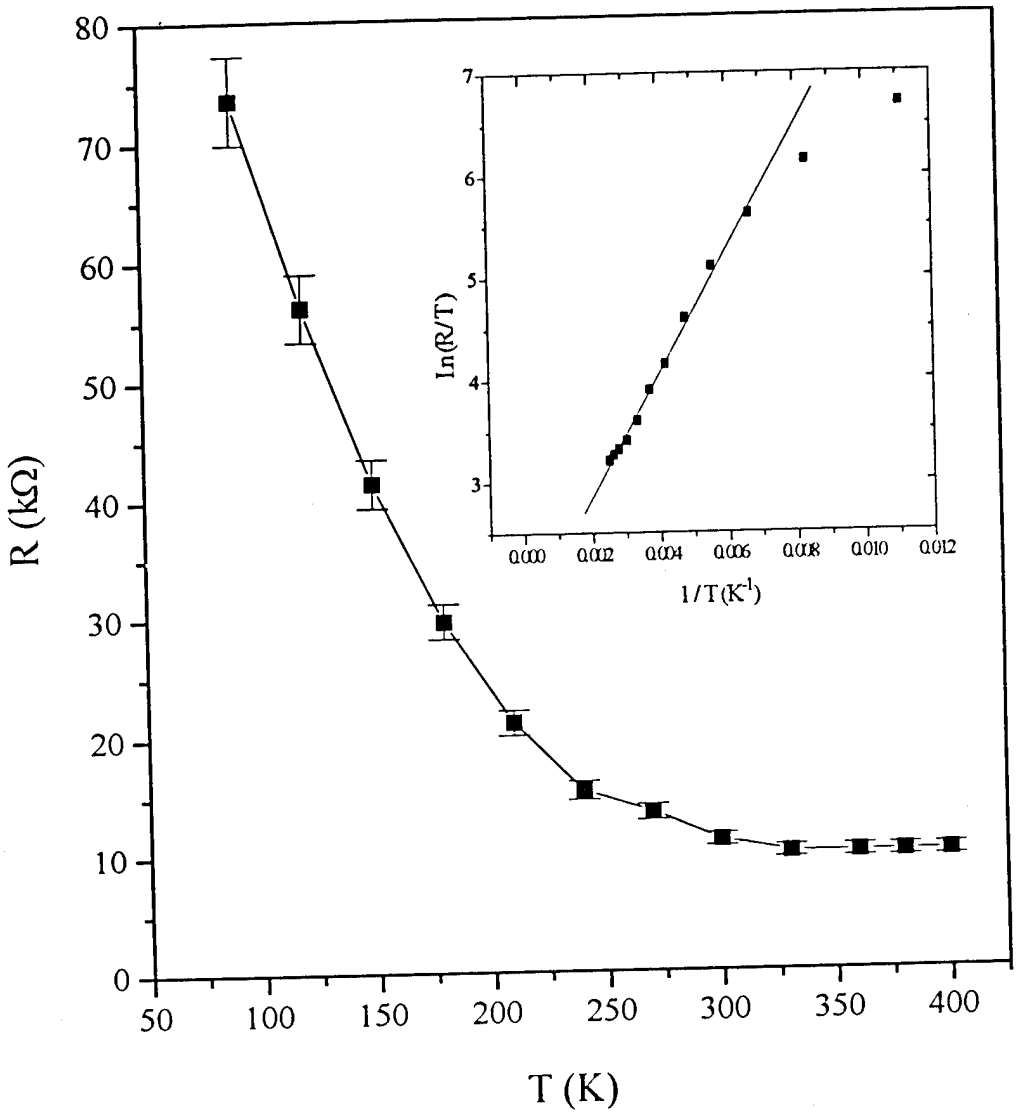

Fig. 4.17: The variation of the feedback resistor, R_f, with temperature. The inset shows that contact resistance mainly dominates the behavior of R_f.

the front end would saturates at about 15 μW of input power (as opposed to 50 μW).

The power dissipated in the pixel which is mainly due to the laser pre-bias at threshold will decrease as a result of the decrease in the threshold current for low temperatures. From Eq. 4.22 and Fig. 4.16 we can predict that the laser dissipated power will decrease from 37 mW to 7 mW as temperature is lowered from 300 K to 77 K, using $P_L=I_{TH}V_L$, and V_L~1.5 V.

At low temperature, the pixel noise will be reduced and its sensitivity improved due to following factors: lower p-i-n dark current will contributeto lowered shot noise, the increase of β in low temperature results in a lower base current (I_b) for a fixed collector current reducing shot noise, increase of HBT transconductance (g_m) at lower temperature will decrease channel noise, and the increase in R_f will reduce Johnson and channel noise. Hence, the overall smart pixel performance will improve at low temperature.

We have calculated the theoretical dependence of pixel sensitivity (P_{min}) and switching energy (E_{sw}) for the smart pixel discussed here using Eq. 4.4. In this calculation, we have included temperature dependencies for the terms in Eq. 4.2 wherever applicable, however, we ignored the temperature dependence of contact resistance and its effect on the value of R_f. The results are plotted in Fig. 4.18. The sensitivity is shown to improve by 2 dB as temperature changes from 300 K to 77 K, resulting in an improvement of 5 fJ (11 fJ down to 6 fJ) in E_{sw} for the same temperature range. This issue will be explored further in Ch. 5.

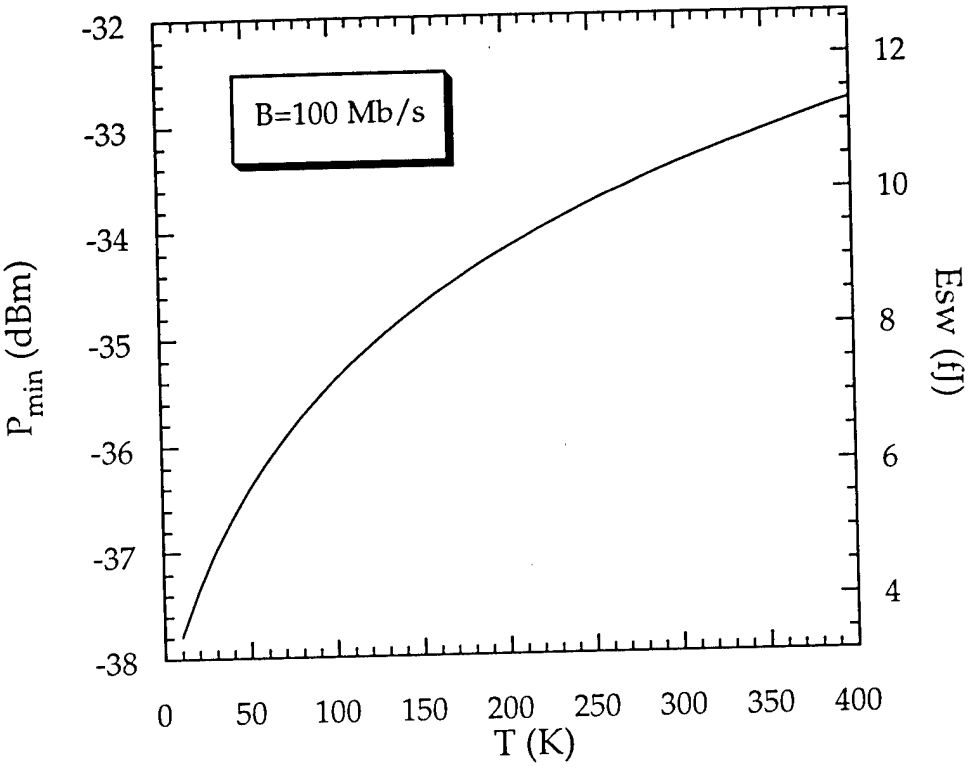

Fig. 4.18 : Sensitivity (P_{min}) and switching energy (E_{sw}) of the smart pixel as a function of temperature.

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Chapter 5

Analysis of Receiver Bandwidth and Temperature Dependence

5.1 Introduction

Receiver sensitivity is a parameter which characterizes the minimum power level that can be detected while maintaining a desired signal-to-noise ratio (in the analog case) or bit error rate (in the digital case). For a given receiver, the sensitivity is not only determined by circuit parameters, but by the bit rate and temperature. At the quantum limit for detection, the receiver sensitivity to achieve a BER=10^{-9} is equivalent to 20 photons/bit[1]. In practice, most receivers operate at 20 dB or more from this limit, due to noise contributed by various elements in the detection scheme[2,3]. This is equivalent to saying that receiver requires at least 1000 photons/bit to achieve a bit error rate (BER) of 10^{-9}. However, as the bandwidth goes up, the bit time slot decreases. Hence to maintain 1000 photons/bit, the bit amplitude must increase, resulting in an increase in the minimum detectable power[4].

Changes in temperature also influence the receiver sensitivity, since they effect the photodetector dark current and other receiver noise terms. Study of temperature effects is not only significant in determining the improvement in sensitivity with device cooling, it is also useful in

predicting sensitivity degradation as a result of device heating due to power dissipation.

In preceding chapters, we discussed the design and performance of an OEIC smart pixel switch using a p-i-n as the photodetector combined with an HBT-based amplifier. In this chapter, we use noise analysis to model the temperature and bit rate dependence of sensitivity for different receiver types. In sections 5.2, we present simulation results on p-i-n based receivers in conjunction with HBT or FET-based amplifiers. In section 5.3, we substitute APD's as the photodetector device of the receivers, and study their performance. In section 5.4, we compare different detection schemes, and in 5.5, we discuss the transmitter noise.

The device and circuit parameters used throughout this chapter are based on experimental values whenever possible. These parameters were measured for both HBT and FET-based monolithically integrated receivers and transmitters. Therefore, the calculations follow the experimental circuit performance.

5.2 P-i-n-based receivers

In general, optical receivers consist of five components: a photodiode to detect the signal, a pre-amplifier as the first stage of amplification, a post-amplifier to provide further amplification, an equalizer to reshape the signal after possible distortions by the preamplifier-post amplifier combination, and a filter to maximize the signal-to-noise ratio while preserving the essential features of the signal. In addition to the noise contributed by the p-i-n, the pre-amplifier as the first stage of amplification is the other significant source of noise added to the signal[5].

Here, our main focus will be on the noise generated by the detector-preamplifier, and its effects on system sensitivity. The post-amplifier noise is ignored assuming that the pre-amplifier gain is high. In total noise calculations, another contribution would come from the signal-induced noise in the photodetector which is a result of the randomness associated with the rate of arrival of the photons at the detector, or the random nature of the avalanche process in APD's. However, in sensitivity calculations, the objective is to find the minimum signal level to achieve a desired BER, and hence the signal-induced noise terms are not included. The noise performance of p-i-n photodetectors in conjunction with HBT or FET pre-amplifiers is discussed in the next section.

5.2.1 P-i-n photodetectors with HBT-based amplifiers

The schematic for a single stage transimpedance amplifier using bipolar transistors is shown in Fig. 5.1. The expressions for noise terms of the p-i-n/HBT case are similar to those presented in Ch. 4, in the smart pixel sensitivity analysis. Here, they are repeated for clarity as follows[5] :

$$
\begin{aligned}
&< i_t^2 >= 2q(I_b + I_d)BI_2, \\
&< i_{ch}^2 >= \frac{2qI_c}{g_m^2}[(\frac{1}{R_f} + \frac{1}{r_{be}})^2 BI_2 + (2\pi C_T)^2 B^3 I_3], \\
&< i_r^2 >= \frac{4kT}{R_f} BI_2, \\
&< i_{rb}^2 >= 4kTr_{bb}[\frac{BI_2}{R_f^2} + (2\pi)^2 (C_d + C_s)^2 B^3 I_3].
\end{aligned}
\qquad (5.1).
$$

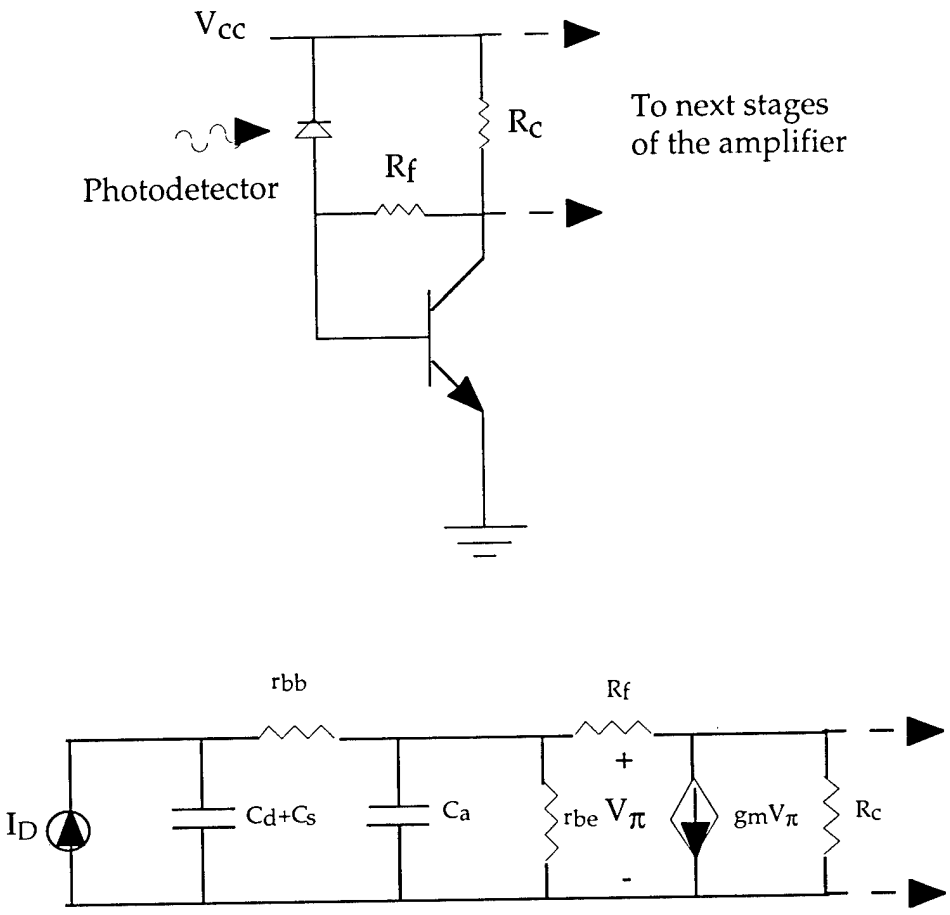


Fig. 5.1 : Schematic of an HBT based transimpedance amplifier and the small signal model.

In Eq. 5.1, q is the electron charge, k is Boltzmann's constant, T is the temperature, B is the data bit rate, I_b is the quiescent base current, I_d is the detector dark current, I_c is the quiescent collector current, g_m is the front end HBT transconductance, R_f is the feedback resistor, r_{be} is the dynamic base-emitter resistance, C_T is the total capacitance due to amplifier (C_a), detector (C_d) and stray capacitance associated with leads and package (C_s), r_{bb} is the base resistance, and I_2 and I_3 are the Personick integrals with values of 0.5 and 0.1, respectively.

The temperature dependence of noise terms in Eq. 5.1 are linear in temperature (T), except for the following parameters:

$$\beta(T) = \beta_0 - \xi T \tag{5.2}$$

is obtained empirically, where β_0 and ξ are constants. Thus:

$$I_b(T) = \frac{I_c}{\beta(T)} \tag{5.3}$$

$$g_m(T) = \frac{qI_c}{kT} \tag{5.4}$$

$$r_{be}(T) = \frac{\beta(T)}{g_m(T)} \tag{5.5}$$

Although achieving optimum sensitivity in receiver design is the basic goal, there are other factors that influence the design. These may in fact result in a receiver with less than the optimum sensitivity. Two such factors are the need for a large dynamic range, and the need for design optimization at high bit rates. As seen in Ch. 2, in the small signal analysis of the smart pixel, the dominant pole of the front end, τ_1, is to a good approximation equal to: $\tau_1 = R_f C_{bc}$, where R_f is the feedback resistor, and C_{bc} is the base-collector junction capacitance of the front-end transistor. To ensure high

bandwidth operation of the amplifier, the value of the feedback resistor needs to be no larger than[4] :

$$R_f = \frac{1}{2\pi C_{bc} B I_2} \tag{5.6}$$

Substituting the value of R_f from Eq. (5.6) into the expression for Johnson noise implies that $\langle i_r^2 \rangle$ is proportional to B^2.

In our best photodiodes, we obtained I_d=2 nA at room temperature. As mentioned in Ch. 4, the dark current of the p-i-n photodiode, I_d, is generally due to a combination of generation-recombination ($I_{d(g\text{-}r)}$) and surface leakage ($I_{d(surf)}$). Although it is not possible to determine the exact contribution of each of the two mechanisms without further study, here, we assume that the surface leakage and generation-recombination mechanisms each make a 50% contribution to the total dark current. The expressions for these currents, as in Ch. 4, are:

$$I_{d(g-r)} = I_{g-r0} T^{3/2} exp(-\frac{\Delta E_a}{kT}) \tag{5.7}$$

$$I_{d(surf)} = I_{s0} T^2 exp(-\frac{\Delta E_a}{kT}) \tag{5.8}$$

$$\text{and, } I_d(T) = I_{d(g\text{-}r)}(T) + I_{d(surf)}(T) \tag{5.9}.$$

Table 5.1 contains the values used for the device parameters in our calculations. These values are based on experimental measurements on the smart pixel circuit. The total noise current for the p-i-n/HBT case, $\langle i_{pb}^2 \rangle$ is:

$$\langle i_{pb}^2 \rangle = \langle i_t^2 \rangle + \langle i_{ch}^2 \rangle + \langle i_r^2 \rangle + \langle i_{rb}^2 \rangle \tag{5.10}.$$

Table 5.1

List of device parameters for the p-i-n/HBT receiver

Parameter	Definition	Value
I_d	total dark current @T=300 K	2 nA
$I_{d(g\text{-}r)}$	g-r part of I_d	1 nA
$I_{g\text{-}r0}$	Y-intercept of $I_{d(g\text{-}r)}(T)$	1 μA
$I_{d(surf)}$	surface recombination part of I_d	1 nA
I_{surf0}	Y-intercept of $I_{d(surf)}(T)$	50 nA
ΔE_a	activation energy (Ref. [4])	0.4 eV
I_c	quiescent collector current	1 mA
β	current gain I_c/I_b @T=300 K	250
β_0	Y-intercept of $\beta(T)$	330
ξ	empirical temperature coeff. of β	0.27 /K
g_m	transconductance (@T=300 K)	0.04 A/V
R_c	external collector resistance	2 kΩ
R_f	feed back resistance (typical range: 0.3-10 kΩ, Ref. [6,7])	$R_f = \frac{1}{2\pi C_{bc} B I_2}$
r_{be}	$r_{be} = \beta/g_m$ (@T300 K)	5.2 kΩ
r_{bb}	base series resistance	1 kΩ
I_b	quiescent base current	4 μA
C_T	total capacitance	1 pF
C_{bc}	base-collector junction capacitance	0.3 pF
C_s	stray capacitance	0.5 pF
C_d	detector capacitance	0.1 pF

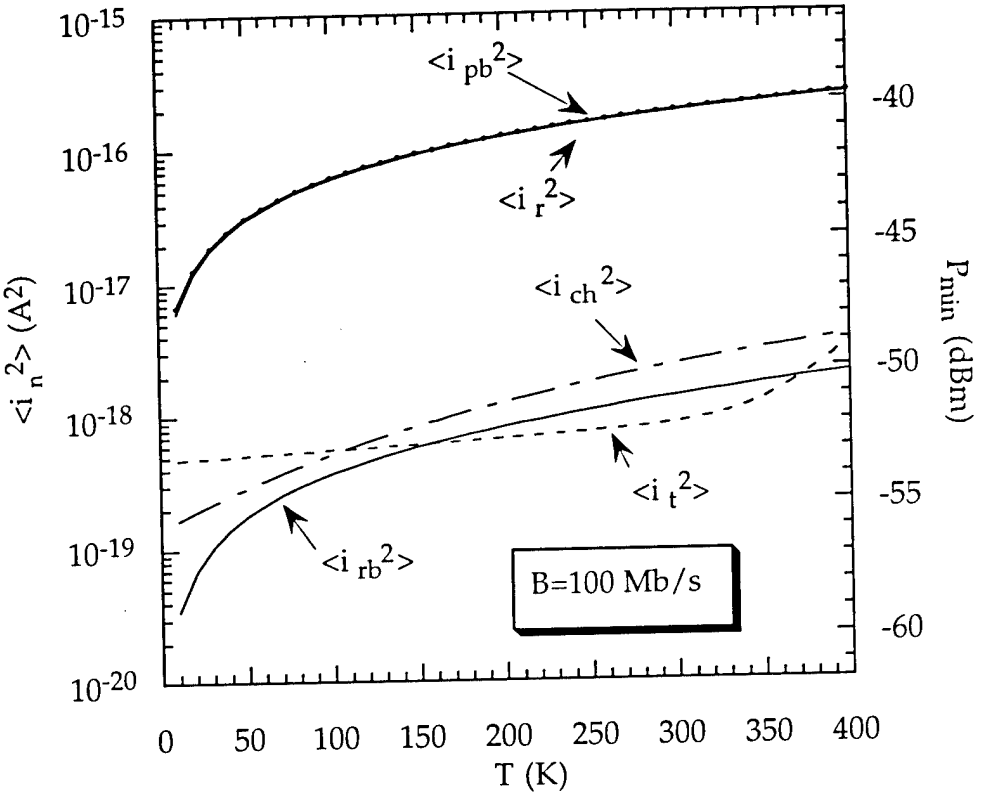
The sensitivity of a receiver is then calculated using:

$$P_{min} = \frac{1+r}{1-r}\frac{Q}{\eta}\left(\frac{hc}{q\lambda}\right) < i_{pb}^2 >^{1/2} \qquad (5.11)$$

where the circuit parameters assumed are given below:

Parameter	Definition	Value
r	extinction ratio ($r=p_0/p_1$)	0
Q	signal/noise ratio	6 (BER=10^{-9})
η	detector efficiency	0.85
λ	operation wavelength	1.3 μm

In Fig. 5.2 the magnitude of each of the noise currents for the p-i-n/HBT receiver has been calculated as a function of temperature for bit rates of (a) 100 Mb/s, (b) 1 Gb/s, and (c) 10 Gb/s. The bit rates chosen correspond to the bandwidth of the smart pixel, and to bit rates of interest in long distance optical communication networks[4]. These plots clearly show that with the specific parameters of our smart pixel, and at its operation bandwidth (B=100 Mb/s for R_f=10 kΩ), the Johnson noise due to R_f ($<i_r^2>$) dominates the noise terms. The temperature (T) dependence of this term is small ($<i_r^2> \sim T$), resulting in a T-dependence for P_{min} as: $P_{min} \sim 0.5\text{Log}(T)$, and hence there is only about a 3 dB improvement by lowering the temperature from T=300 K down to T=77 K. At larger bandwidths (lower R_f) the other noise terms become more significant, which is also related to the B^3-dependence of $<i_{ch}^2>$ and $<i_{rb}^2>$ terms, in contrast to the linear dependence of $<i_r^2>$ on bit rate. Channel noise ($<i_{ch}^2>$) nearly matches $<i_r^2>$ at B=10 Gb/s. This term



(a)

Fig. 5.2: Noise currents as a function of temperature for a p-i-n/HBT receiver for bandwidth of (a) 100 Mb/, (b) 1 Gb/s and (c) 10 Gb/s. The total noise current is $\langle i_{pb}^2 \rangle$ and it is the sum of shot noise $\langle i_t^2 \rangle$, channel noise $\langle i_{ch}^2 \rangle$, and Johnson noise terms due to the feedback resistor $\langle i_r^2 \rangle$, and the base resistance $\langle i_{rb}^2 \rangle$.

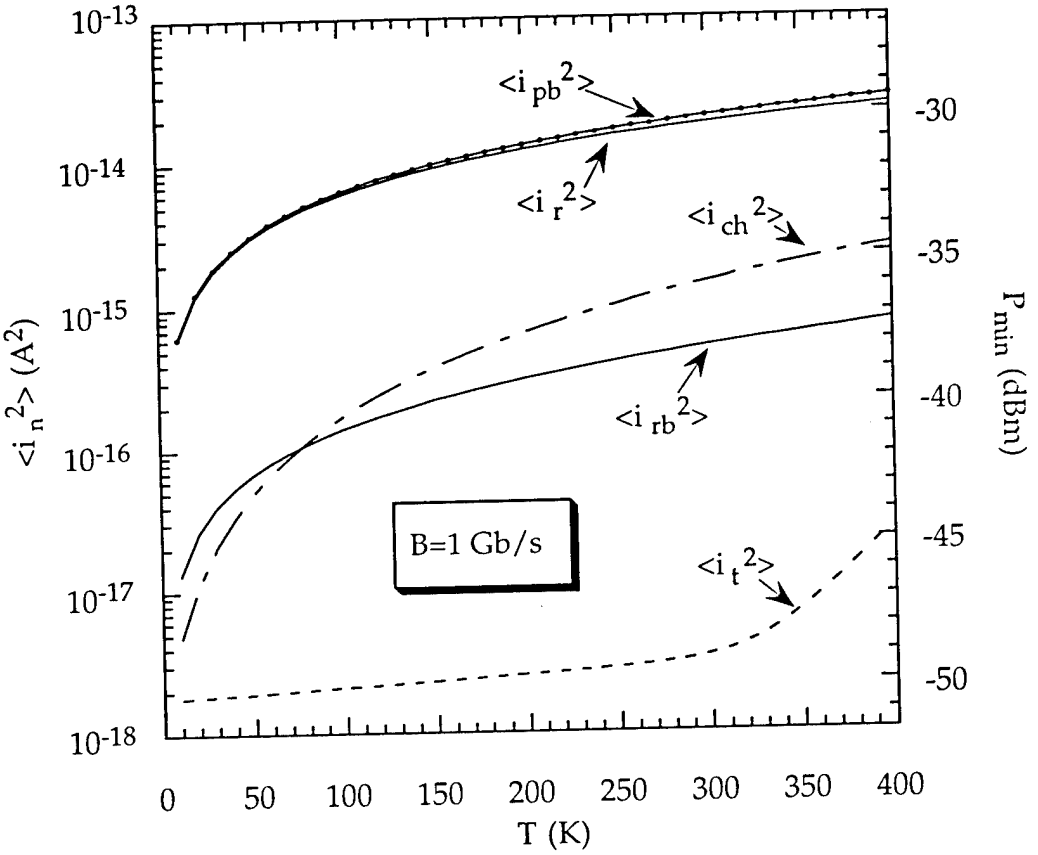

10-13
10-14
10-15
10-16
10-17
10-18
<i n2> (A2)
<i pb2>
<i r2>
<i ch2>
<i rb2>
<i t2>
B=1 Gb/s
-30
-35
-40
-45
-50
Pmin (dBm)
0
50
100
150
200
250
300
350
400
T (K)

Fig. 5.2 (b)

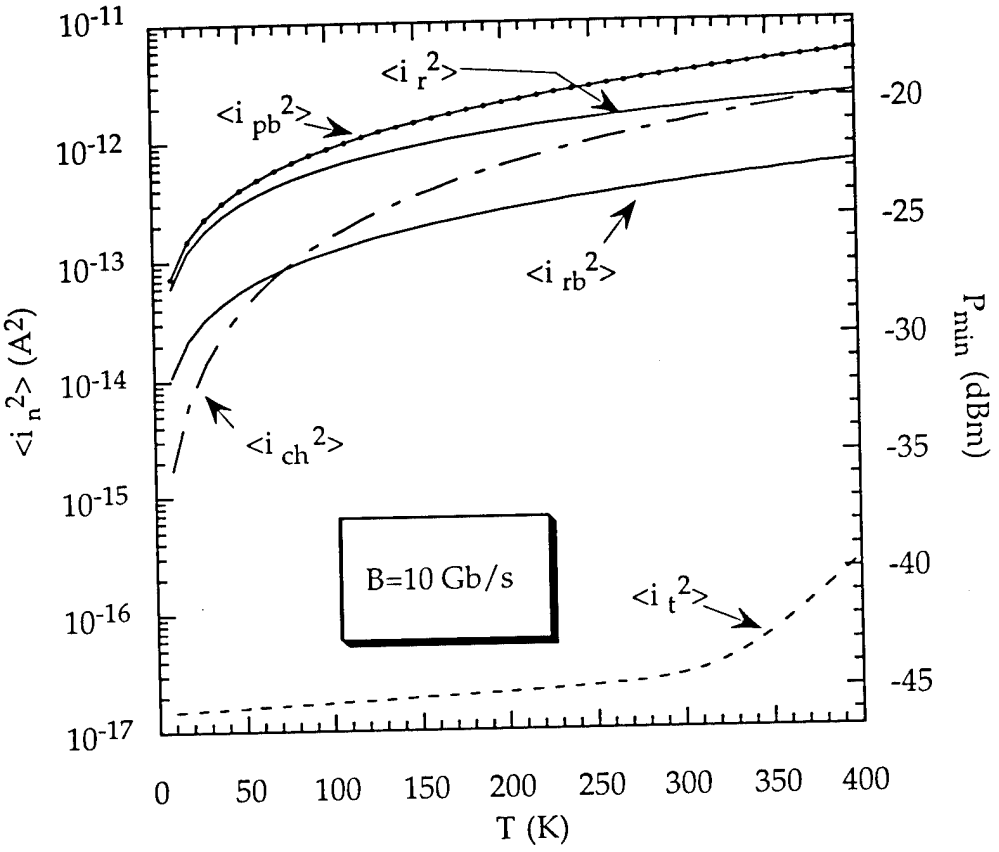

10-11
10-12
10-13
10-14
10-15
10-16
10-17
<in2> (A2)
-20
-25
-30
-35
-40
-45
Pmin (dBm)
<ir2>
<ipb2>
<irb2>
<ich2>
<it2>
B=10 Gb/s
0
50
100
150
200
250
300
350
400
T (K)

Fig. 5.2 (c)

shows a stronger temperature dependence ($<i_{ch}^2>\sim T^2$), and hence there is about a 5 dB improvement in sensitivity in the temperature range discussed.

In the case of shot noise, the low temperature value is dominated by I_b, and hence it has a weak temperature dependence. At higher temperature, dark current increases and eventually dominates for T>300 K. However, the contribution of shot noise to the total noise current ($<i_{pb}^2>$) is relatively insignificant. In the next section, sensitivity of a receiver using a FET is discussed and compared to that of an HBT-based front end.

5.2.2 P-i-n photodetectors with FET amplifiers

The schematic for a receiver and FET amplifier is shown in Fig. 5.3. The configuration corresponds to a high-impedance (HZ) front end, for which experimental data were obtained in our group[10]. However, the treatment that follows can also be applied to a transimpedance (TZ) amplifier by replacing R_l with the feedback resistor, R_f, in the noise terms[4] in Eq. 5.12. Here, we have considered an InP FET device. The noise current terms for this configuration include shot noise ($<i_t^2>$), Johnson noise in the feedback resistor ($<i_r^2>$), channel noise due to the channel conductance $<i_{ch}^2>$, and FET 1/f noise ($<i_{fc}^2>$). Eq. 5.12 contains the expression for each of these terms:

$$
\begin{aligned}
&< i_t^2 >= 2q(I_g + I_d)BI_2, \\
&< i_{ch}^2 >= \frac{4kT\,\Gamma}{g_m}[(\frac{BI_2}{R_l^2} + (2\pi C_T)^2 B^3 I_3], \\
&< i_r^2 >= \frac{4kT}{R_l} BI_2, \\
&< i_{fc}^2 >= \frac{4kT\,\Gamma}{g_m}[\frac{BI_2}{R_l^2} + (2\pi C_T)^2 f_c B^2 I_f].
\end{aligned}
\qquad (5.12)
$$

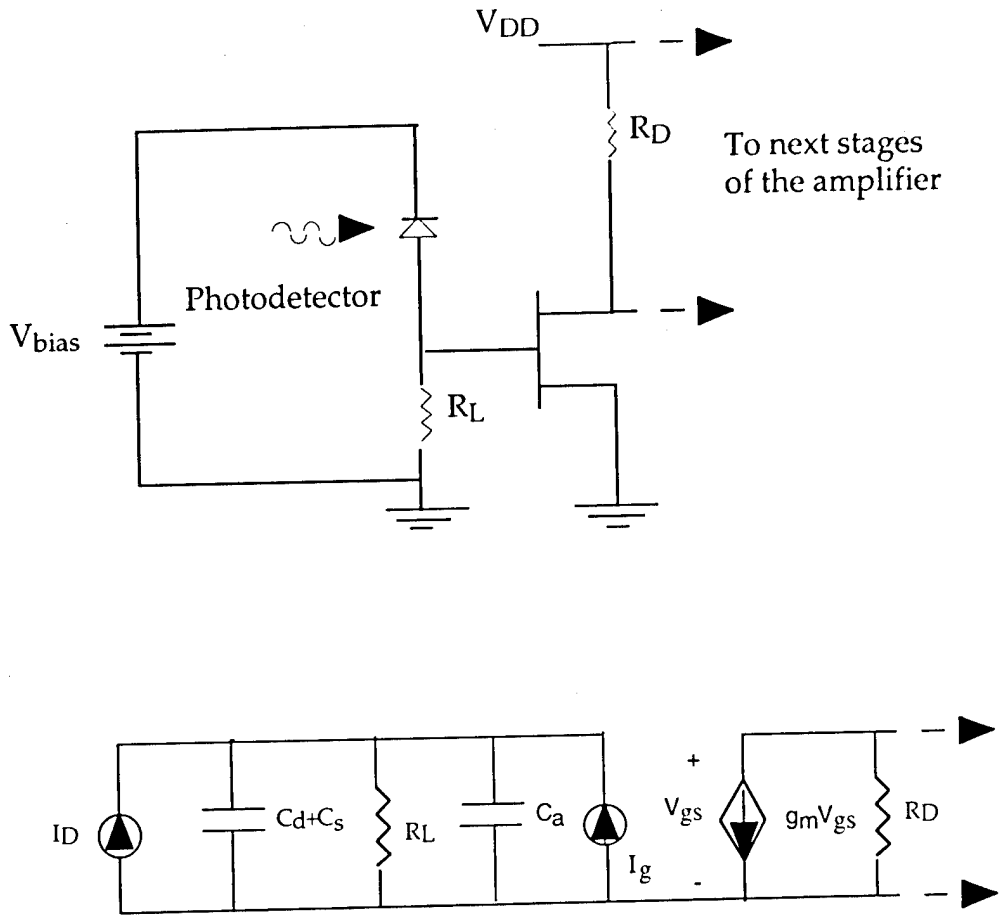


Fig. 5.3: Schematic of the front end of a p-i-n/FET amplifier.

In Eq. 5.12, I_g is the gate leakage current, Γ is the excess noise factor of the FET, g_m is the transconductance measured at the amplifier operating point, I_f is the effective receiver bandwidth integral, and f_c is the FET 1/f noise corner frequency. The transconductance of a FET operating under strong saturation can be approximated by[8]:

$$g_m \approx \varepsilon_s v_p Z/W_c \approx v_p Z\{\varepsilon_s q N_D/[2(V_{bi}-V_{GS})]\}^{1/2} \qquad (5.13)$$

where ε_s is the permitivity of the semiconductor, Z is the gate width, W_c is the depletion width, N_D is the donor concentration, V_{bi} is the built in potential and V_{GS} is the gate-source voltage. The parameter, v_p, is the peak carrier drift velocity defined as $v_p(T) = E\mu(T)$, where μ is the electron mobility and E is the electric field. Thus the temperature dependence of v_p is due to μ, and using the same argument as in Ch. 4, we conclude $v_p \sim T^{-2}$. We ignore the temperature dependence of the other terms in Eq. 5 as they are small compared to v_p. Hence, $g_m = g_{m0}T^{-2}$, where g_{m0} is a constant whose value has been obtained from the data.

The dark current, as in Eq. 5.9, is assumed to be the sum of generation-recombination, and surface leakage. The expressions and parameter values for $I_{d(g\text{-}r)}$ and $I_{d(surf)}$ are the same as those given in Eq. 5.7 and Eq. 5.8. The mechanisms contributing to gate leakage current are: generation-recombination, surface leakage[9], and band-to-band tunneling at the gate-drain junction[10]. Here, we assume a general case where each of these three mechanisms contribute equally to the measured gate current. Each term can be expressed as[11]:

$$I_{d(g-r)} = I_{g-r0}T^{3/2}\exp(-\frac{\Delta E_{ag}}{kT}) \qquad (5.14)$$

$$I_{d(surf)} = I_{s0}T^{2}\exp(-\frac{\Delta E_{ag}}{kT})$$

$$I_{tun} = \gamma A \exp(-\frac{\Theta m_0^{1/2} E_g^{3/2}}{q\hbar E_m}) \qquad (5.15)$$

and $I_g(T) = I_{g(g\text{-}r)}(T) + I_{g(surf)}(T) + I_{g(tun)}(T)$. In Eq. 5.14, ΔE_{ag} is the activation energy for gate leakage[12]. In Eq. 5.15, A is the device area, m_0 is the free

electron mass, $\hbar$ is Planck's constant divided by 2π, E_g is the band gap, and E_m is the maximum junction electric field given by $E_m=-2(V+V_{bi})/W$, where W is the depletion region width. The parameter Θ is a dimensionless quantity given by $\Theta=\alpha(m_c^*/m_0)^{1/2}$, where m_c^* is the effective mass of the electron, and α depends on the shape of the tunneling barrier, and is on the order of unity for band-to-band processes. The temperature dependence of E_g can be written as[13]:

$$E_g(T) = E_0 - \frac{\varpi T^2}{\zeta + T} \tag{5.16}$$

where ζ and ϖ are constants[14]. The prefactor γ depends on the initial and final states of the tunneling barrier and for band-to-band tunneling is equal to:

$$\gamma = [2m_c^*/E_g]^{1/2}(q^3E_mV/4\pi^2\hbar^2). \tag{5.17}$$

In order to optimize the frequency response of the circuit, similarly to the p-i-n/HBT case, we need to adjust the load resistance, R_l, with bandwidth B as[4]:

$$R_l = \frac{1}{2\pi B I_2 C_T / A_v} \tag{5.18}$$

where A_v is the voltage gain, and has been assumed to be about 3, which corresponds to experimental results[10] for InP FET's with channel doping, $N_D \sim 10^{17}$ cm^{-3}. The values for the parameters are given in Table 5.2.

Similarly to the p-i-n/HBT case, the sensitivity of the p-i-n/FET can be calculated using:

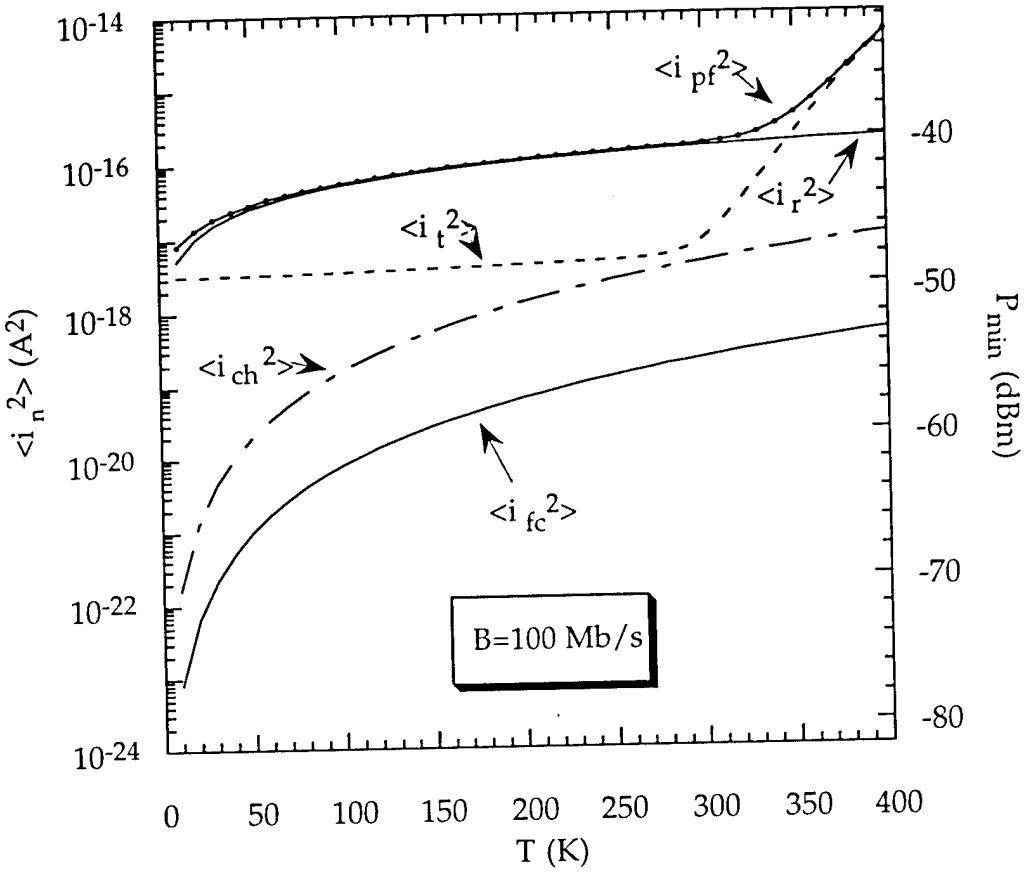
$$P_{min} = \frac{1+r}{1-r}\frac{Q}{\eta}\left(\frac{hc}{q\lambda}\right) < i_{pf}^2 >^{1/2} \tag{5.19}$$

where the circuit parameters are the same as those used in Eq. 5.11. The

Table 5.2

List of device parameters for p-i-n-FET receiver

Parameter	Definition	Value
ΔE_{ag}	activation energy for InP channel	0.7 eV
A	device area	10^{-4} cm^2
ζ	(coefficients of E_g temperature	162 K
ϖ	dependence)	3.6×10^{-4} eV/K
I_g	total gate current @T=300 K	1 μA
$I_{g(tun)}$	tunneling portion of I_g	0.33 μA
$I_{g(g\text{-}r)}$	g-r portion of I_g	0.33 μA
I_{g0}	Y-intercept of $I_{g(g\text{-}r)}$	12 A
$I_{g(surf)}$	surface leakage portion of I_g	0.33 μA
I_{s0}	Y-intercept of $I_{g(surf)}$	0.7 A
Γ	excess noise current	1.5
g_m	transconductance @T=300 K	0.012 S
g_{m0}	$g_m=g_{m0}/T^2$	1080 S/K^2
R_l	load resistance	$R_l = \frac{1}{2\pi B I_2 C_T / A_v}$
	(typical range: 10^3-10^6 Ω, Ref. [4])	
m_c^*/m_0	InP electron effective mass ratio (Ref. [15])	0.08
A_v	voltage gain (Ref. [10])	3
C_T	total capacitance	1 pF
f_c	noise corner frequency (Ref. [4])	25 MHz
I_f	receiver bandwidth integral (Ref. [4])	0.12



(a)

Fig. 5.4: Noise currents for a p-i-n/FET receiver as a function of temperature for different values of bandwidth (a) B=100 Mb/s, (b) B=1 Gb/s, and (c) B=10 Gb/s. The total noise current is $\langle i_{pf}^2 \rangle$ and it is the sum of shot noise $\langle i_t^2 \rangle$, channel noise $\langle i_{ch}^2 \rangle$, Johnson noise due to the load resistor $\langle i_r^2 \rangle$, and the 1/f noise $\langle i_{fc}^2 \rangle$.

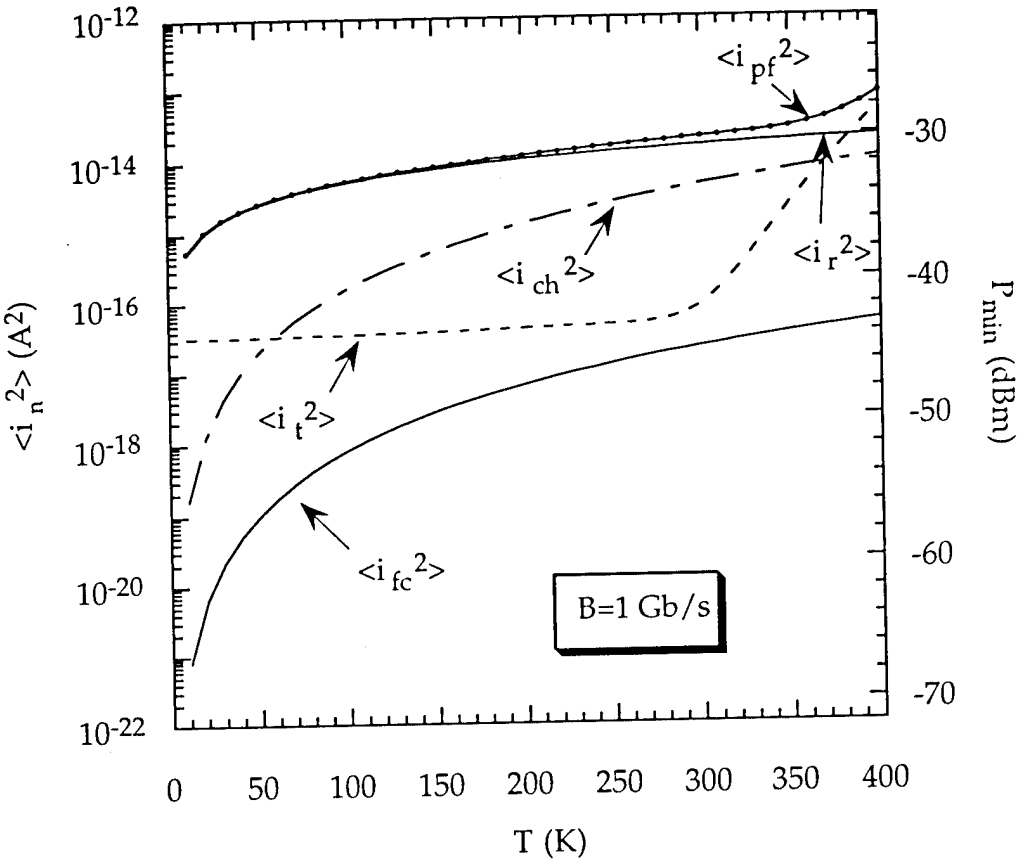
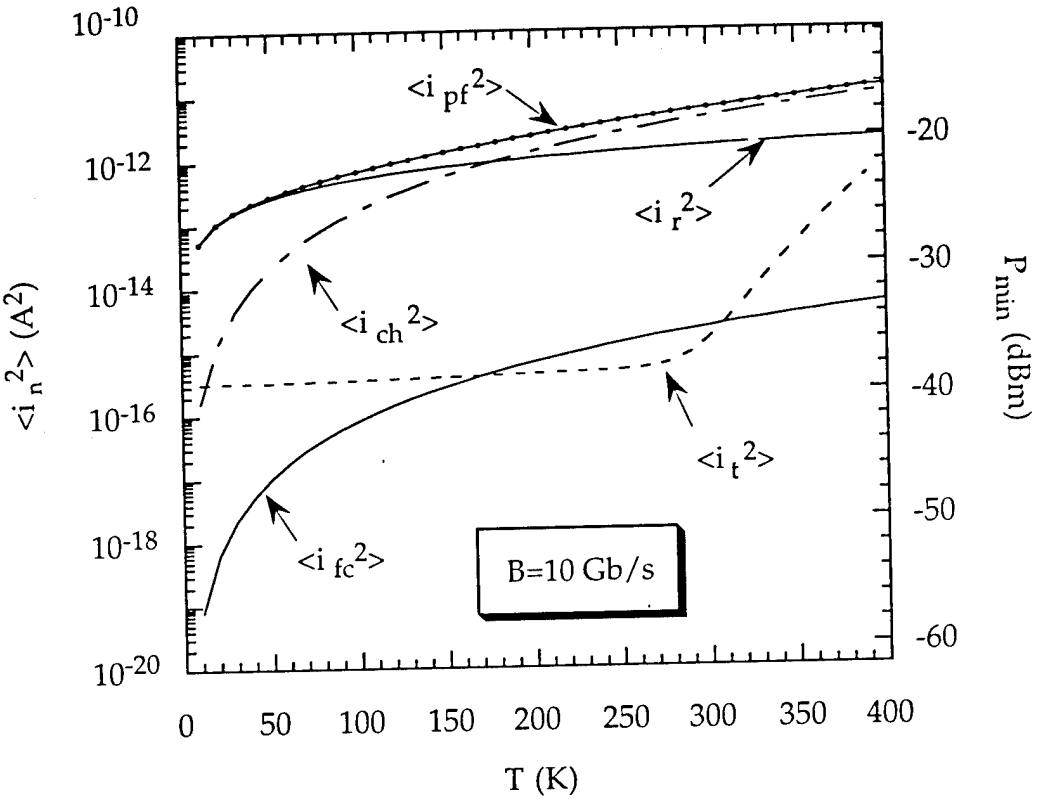

10^{-12}
10^{-14}
10^{-16}
10^{-18}
10^{-20}
10^{-22}
$\langle i_n^2 \rangle$ (A²)
$\langle i_{pf}^2 \rangle$
$\langle i_{ch}^2 \rangle$
$\langle i_r^2 \rangle$
$\langle i_t^2 \rangle$
$\langle i_{fc}^2 \rangle$
B=1 Gb/s
-30
-40
-50
-60
-70
P_{min} (dBm)
0
50
100
150
200
250
300
350
400
T (K)

Fig. 5.4 (b)


10-10
10-12
10-14
10-16
10-18
10-20
<i n2> (A2)
<i pf2>
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<i ch2>
<i t2>
<i fc2>
B=10 Gb/s
-20
-30
-40
-50
-60
Pmin (dBm)
0
50
100
150
200
250
300
350
400
T (K)

Fig. 5.4 (c)

where the circuit parameters are the same as those used in Eq. 5.11. The values of noise currents are calculated and plotted in Fig. 5.4 as a function of temperature for 100 Mb/s, 1 Gb/s, and 10 Gb/s.

Let us first consider T<300 K in Fig. 5.4. In this temperature range, and for B≤1 Gb/s, Johnson noise due to the load resistor ($\langle i_r^2 \rangle \sim T$) dominates the total noise ($\langle i_{pf}^2 \rangle$), and accounts for the weak temperature dependence. Also, shot noise ($\langle i_t^2 \rangle$) is dominated by gate band-to-band tunneling current, and also has a weak T-dependence. At higher bit rates, $\langle i_t^2 \rangle$ and $\langle i_r^2 \rangle$ contribute less to $\langle i_{pf}^2 \rangle$ due to their linear B-dependence (as opposed to the B^3 dependence of others). For B>1 Gb/s, channel noise becomes more significant ($\langle i_{ch}^2 \rangle \sim T^3$), and thus there is a bigger advantage (4 dB) in cooling the sample (as compared to the low bit rates, and the p-i-n/HBT case where $\langle i_{ch}^2 \rangle \sim T^2$).

For T>300 K, $\langle i_t^2 \rangle$ increases due to the exponential temperature dependence of $I_{(g\text{-}r)}$ and $I_{(surf)}$ in both the gate current and the dark current. The sharp increase of $\langle i_t^2 \rangle$ at high temperatures has a larger impact on $\langle i_{pf}^2 \rangle$ at low bit rates, and is essentially insignificant for B=10 Gb/s where $\langle i_{ch}^2 \rangle$ is the most dominant noise term. The shot noise $\langle i_t^2 \rangle$ can be reduced by passivation of the surface and improving the sample quality, hence reducing surface and bulk recombination centers.

Fig. 5.5 shows the minimum sensitivities for the p-i-n/HBT and the p-i-n/FET case as a function of temperatures for different values of bandwidth. They are nearly identical for B<1 Gb/s and T<300 K, and our choice of parameters. Furthermore, they have similar dependencies on temperature. This is expected, as the most dominant terms in that regime and for both cases are the Johnson noise due to R_f (for the p-i-n/HBT case) and R_l (for the

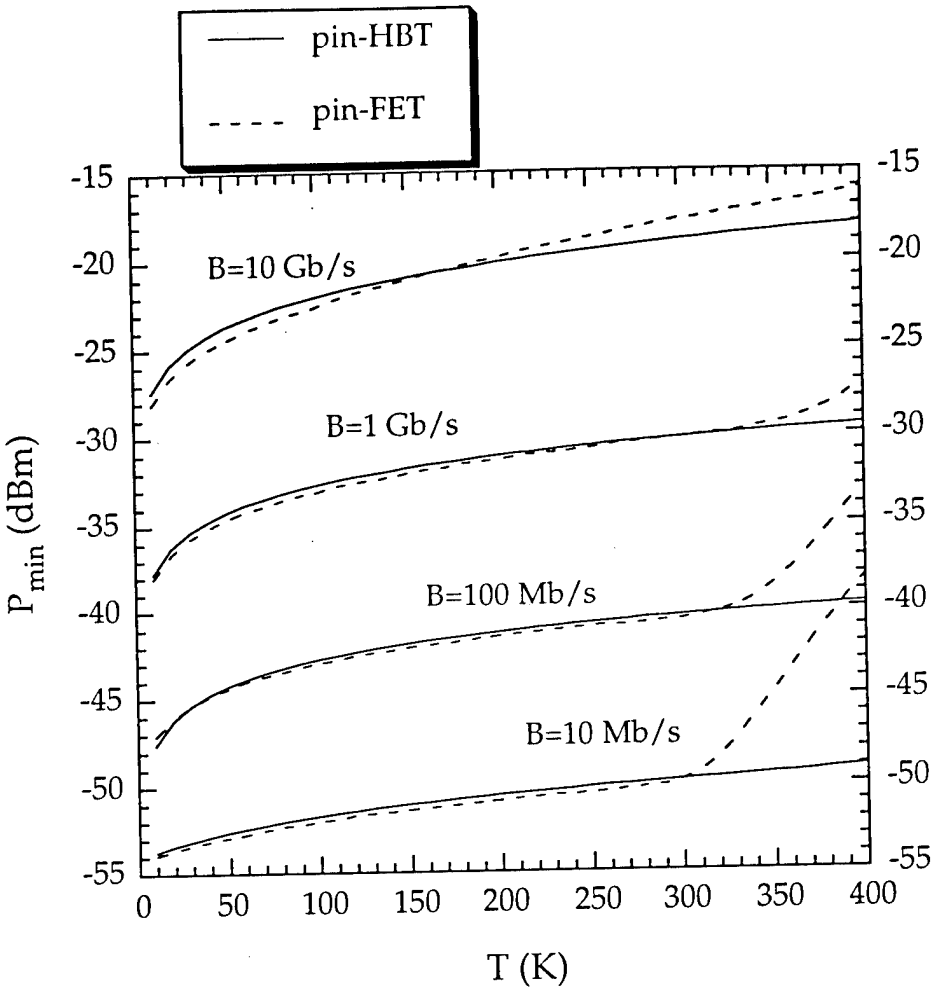


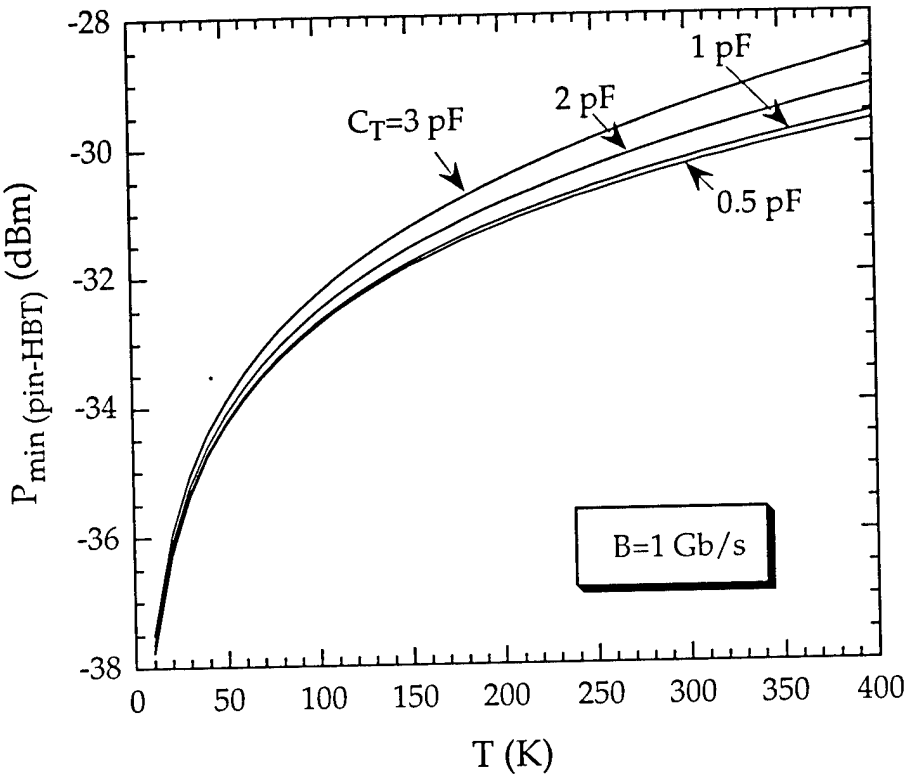
Fig. 5.5: Minimum detectable power (P_{min}) as a function of temperature for different values of bandwidth. The solid line is for a p-i-n/HBT and dotted line is for a p-i-n/FET receiver.

p-i-n/FET case). This indicates a tradeoff in setting the value of R_f and R_l for the cases studied. While low values of these resistors are required for optimizing the high bit rate operation, this is at the expense of reduced sensitivity, and smaller dynamic range.

For T>300 K and B<1 Gb/s, shot noise in p-i-n/FET (which is larger than the p-i-n/HBT due to the gate current) dominates, and thus the improvement of P_{min} at lower temperate is more prominent. Namely, while there is a 12 dB improvement at B=100 Mb/s, this improvement is only about 9 dB at B=10 Gb/s for T changing from 400 K to 77 K.

In the p-i-n/HBT case, there is about a 2 dB improvement for temperature changing from 400K to 77K. Below T=300 K, cooling is most effective in improving P_{min} for higher bit rates in both receiver types, as channel noise dominates. It was mentioned earlier that $\langle i_{ch}^2 \rangle \sim T^2$ for p-i-n/HBT and $\langle i_{ch}^2 \rangle \sim T^3$ for p-i-n/FET circuits. That accounts for the difference seen in P_{min} at B=10 Gb/s for these two receiver types.

In order to examine the effects of device parameters on the sensitivity of the p-i-n/HBT receiver , we have calculated P_{min} for different values of C_T, and plotted the results in Fig. 5.6 (a). Note that we have assumed $C_T=C_{bc}+C_d+C_s$ where the definitions and values are given in Table 5.1. In changing C_T, we have assumed that C_{bc} (and hence R_f) remains constant. It can be seen that at T=300 K, P_{min} improves by about 2 dB as C_T is changed from 3 to 0.5 pF at B=1 Gb/s. Fig. 5.6 (b) shows that changing C_{bc} has a larger impact on sensitivity, namely for C_{bc}: 600-300 fF, there is an improvement of 4 dB in P_{min}. This is expected since in the p-i-n/HBT case, Johnson noise due to R_f dominates the total noise at B=1 Gb/s and R_f is inversely proportional to C_{bc}. For p-i-n/FET, as seen in Fig. 5.7, there is an improvement of 6 dB at



(a)

Fig. 5.6 (a) : Minimum detectable power (P_{min}) for p-i-n/HBT as a function of temperature for different values of total capacitance (C_T), (b) P_{min} as a function of temperature for changing collector-base junction capacitance (C_{bc}).

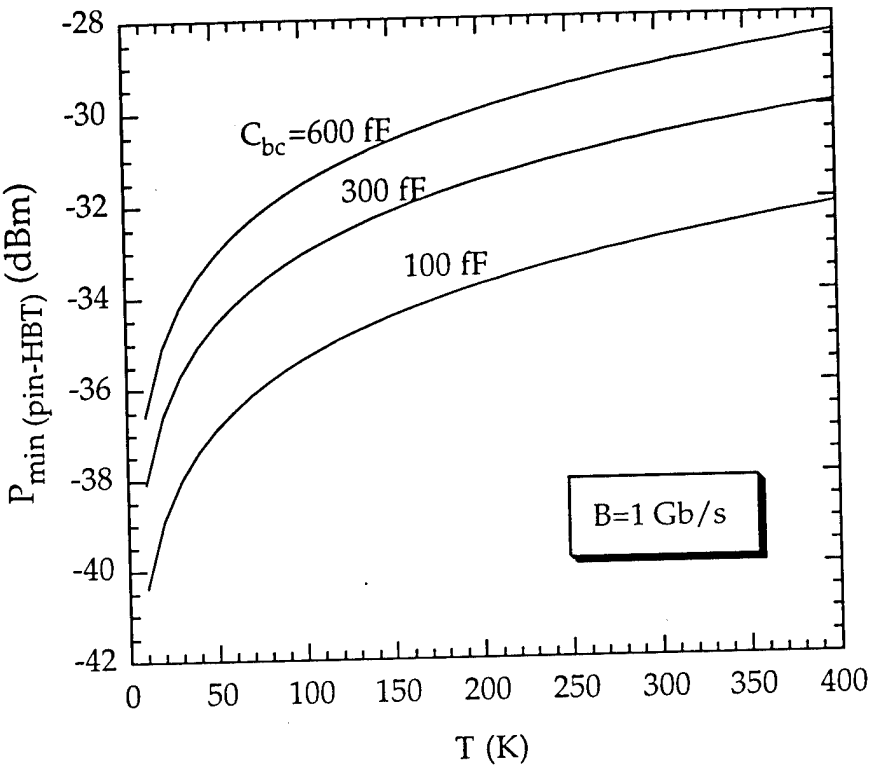

-28
-30
-32
-34
-36
-38
-40
-42
P_{min} (pin-HBT) (dBm)
C_{bc}=600 fF
300 fF
100 fF
B=1 Gb/s
0
50
100
150
200
250
300
350
400
T (K)

Fig. (5.6) (b)

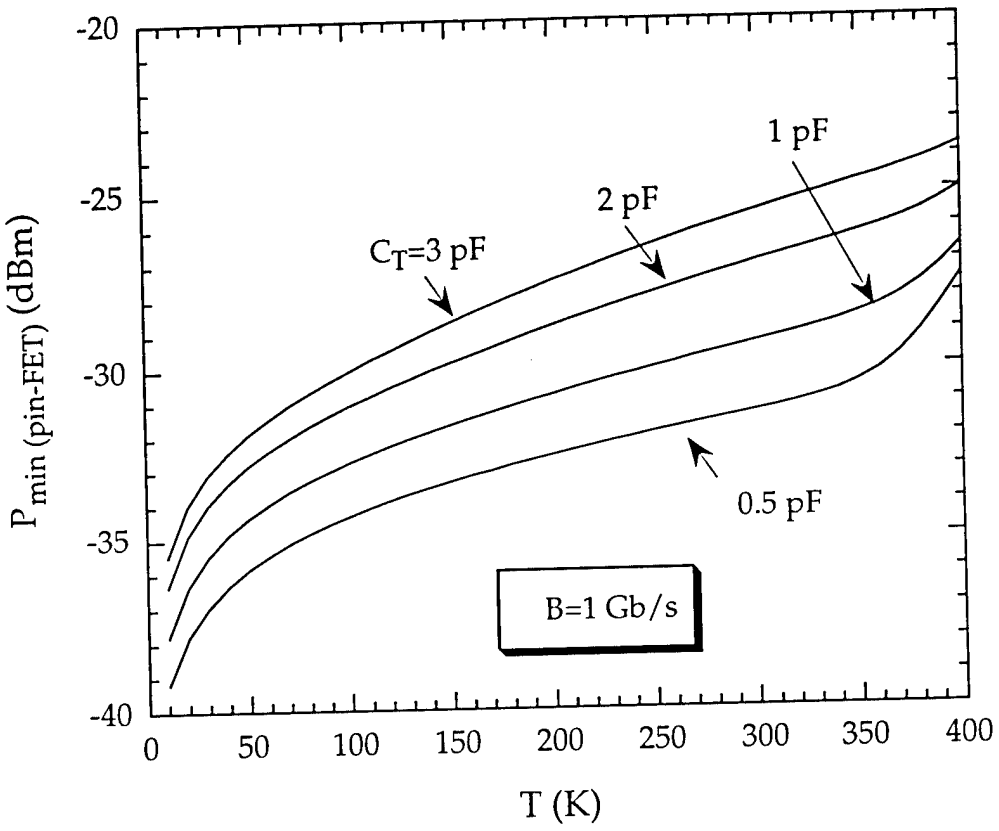


Fig. 5.7: Minimum detectable power (P_{min}) for p-i-n/FET as a function of temperature for different values of total capacitance (C_T).

T=300 K and B=1 Gb/s for C_T: 3-0.5 pF. The increase in this improvement compared to the p-i-n/HBT case is expected, since a reduction in C_T improves sensitivity not only via channel noise (which for this configuration is relatively higher than the pin/HBT), but also through the Johnson noise term (R_l is inversely proportional to C_T).

5.3 APD receivers

In order to improve receiver sensitivity, detectors with gain have been studied extensively. Among such detectors are phototransistors[16], avalanche photodiodes (APD's)[11] and high speed photoconductors[17]. APD's are especially desirable, since they operate under reverse bias, and can therefore demonstrate high speed response with relatively low dark currents[4].

The relatively small band gap of InGaAs makes it a suitable material for long wavelength communication applications. However, this small band gap gives rise to large tunneling current in InGaAs APD's. In the 1980s, separate absorption/multiplication(SAM) devices were fabricated using InGaAs/InP heterostructures[11,18]. In these devices, absorption takes place in the narrow gap InGaAs layer with low electric field, while multiplication in the presence of a high electric field takes place in the wide gap InP layer.

There are several reports for various APD structures made of InGaAs related compounds that attribute the dark current to surface leakage, or generation-recombination[11]. Only the latter type of dark current flows through the bulk and undergoes the avalanche process. Due to the multiplication gain, the contribution of the unmultiplied dark currents to

the noise are in general negligible in comparison with the multiplied dark currents (I_{dm}).

5.3.1 APD based receivers with $I_{dm}=0$

We first consider the case of APD's with zero multiplied dark current, $I_{dm}=0$, implying that only surface effects contribute to the dark current. The purpose for including this case is to obtain a basis for comparison so as to determine the temperature at which the sensitivities for the $I_{dm}=0$ and $I_{dm}\neq 0$ cases are identical, i.e. the regime where the multiplication of the bulk dark current does not degrade the receiver performance.

It is useful to describe the minimum required power for an APD detector in terms of the p-i-n power[4] :

$$\eta P_{min(APD)} = (\frac{\eta P_{min(pin)}}{M}) + (\frac{hc}{\lambda})Q^2F(M)I_1B \qquad (5.20)$$

where M is the multiplication factor, and F(M) is the excess noise factor due to the randomness of the avalanche gain, namely[19]:

$$F(M)=\frac{<M^2>}{<M>^2} \qquad (5.21).$$

To evaluate Eq. 5.20 we use the approximate expression of McIntyre for the excess noise factor[20]. Thus:

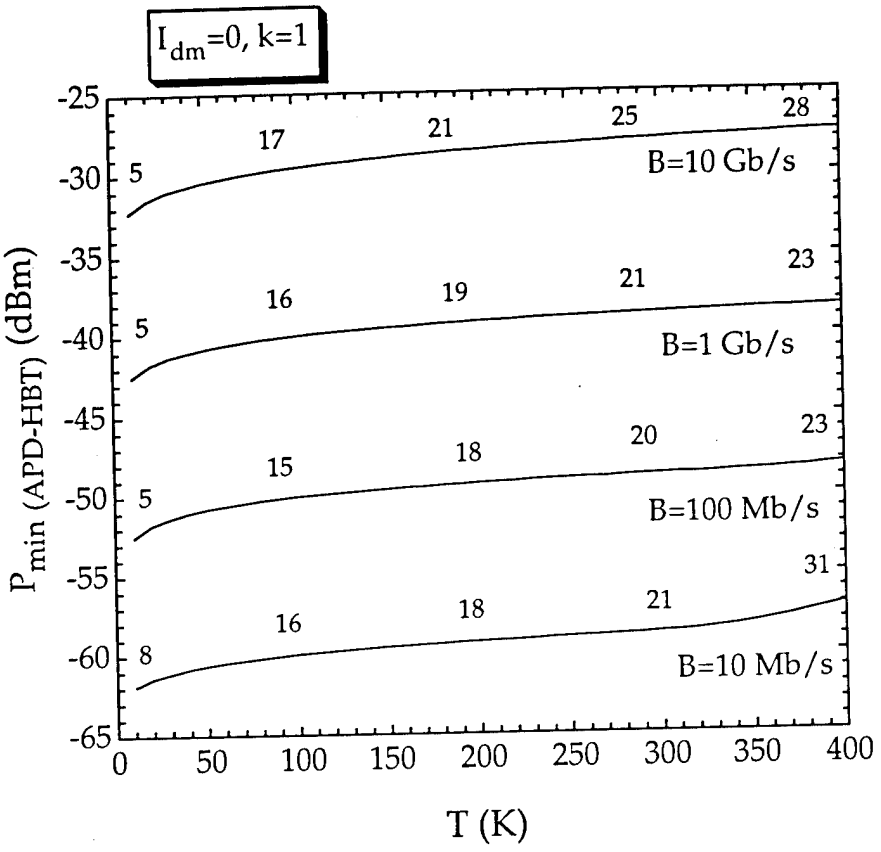
$$F(M) = M\{1-(1-k)[\frac{(M-1)}{M}]^2\} \qquad (5.22).$$

With α and β as the electron and hole ionization coefficients, respectively, the ionization coefficient $k\leq 1$ is defined as: $k = \frac{\alpha}{\beta}$ or $\frac{\beta}{\alpha}$ depending on which carrier initiates ionization. The value of k varies for different

materials: k=1 for Ge and GaAs, k=0.5 for InP, and k=0.025 for Si. Smaller values of k are desirable, since for large k, a feedback process exists in which any slight fluctuation in the electron multiplication process is fed back and amplified because of the hole initiated impact ionization. This results in an increase in the length of the electrical pulse, which could eventually give rise to gain-bandwidth-product limitations. However, if only one carrier is involved in impact ionization (k<<1), the avalanche proceeds only in one direction, the feedback does not exist, and excess noise is greatly reduced[21].

Supperlattice (SL) APD's[22] and stair case APD's[23] are among the proposed structures that reduce the effective value of k. In SL-APD's fabricated using InGaAsP/$In_{0.52}Al_{0.48}As$ or InGaAs/InAlAs, the energy bands line up such that ΔE_v is reduced (ΔE_v=0.03 eV and 0.22 eV for the above structures, respectively) while ΔE_c is still significant (ΔE_c=0.39 eV and 0.47 eV, respectively)[22]. As the electron flows across the heterojunction, it gains kinetic energy from the large conduction band discontinuity, and will be more likely to cause impact ionization. However, holes will have no chance of gaining kinetic energy, or will gain a smaller amount of energy. The enhanced magnitude of α compared to β, will help reduce the value of k to about 0.05[24].

We have used Eq. 5.20 to obtain sensitivity for APD/FET and APD/HBT configurations, using the P_{min} values obtained in Eqs. 5.11 and 5.19. The calculations are performed for k=1, 0.5, and 0.025. Results are plotted in Fig. 5.8 (a), (b), (c) for APD/HBT and in Fig. 5.9 (a), (b), (c) for APD/FET. It can be seen for both APD/HBT and APD/FET cases the sensitivities are very close. Furthermore, for both cases, the sensitivity



(a)

Fig. 5.8: Receiver sensitivity as a function of temperature for different values of bandwidth for an APD/HBT receiver for I_{dm}=0 and (a) k=1, (b) k=0.5, and (c) k=0.025. The values for the avalanche gain that minimizes the required power, M_{opt}, are given next to each line.

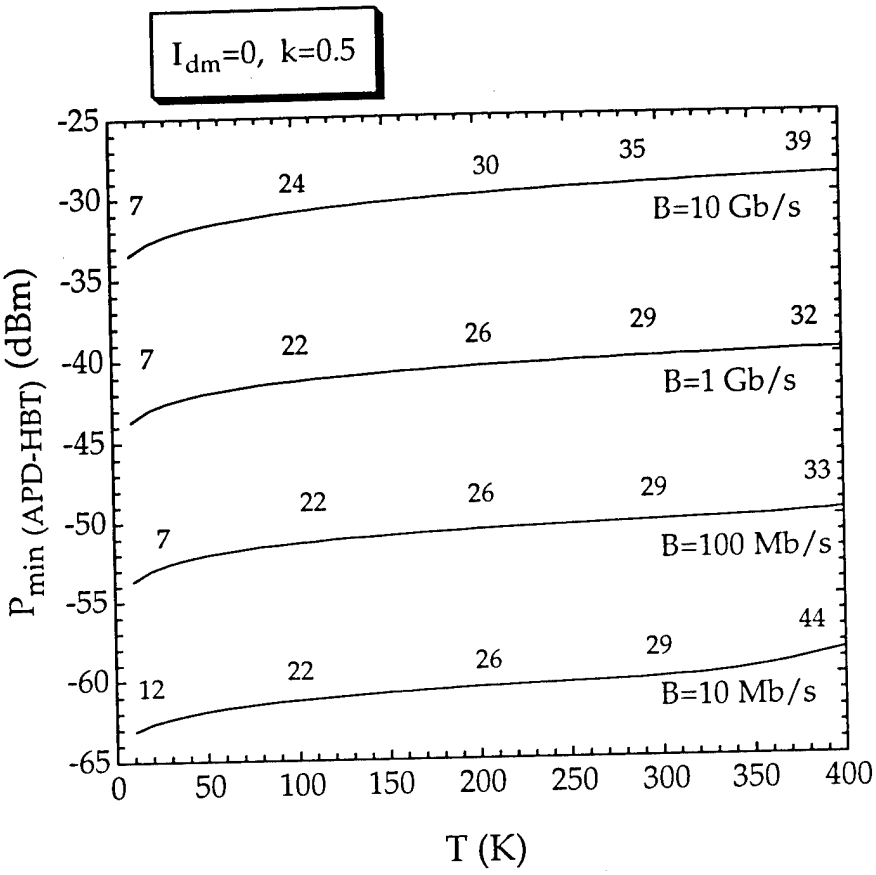

I_{dm}=0, k=0.5
-25
-30
-35
-40
-45
-50
-55
-60
-65
P_{min} (APD-HBT) (dBm)
0
50
100
150
200
250
300
350
400
T (K)
7
24
30
35
39
B=10 Gb/s
7
22
26
29
32
B=1 Gb/s
7
22
26
29
33
B=100 Mb/s
12
22
26
29
44
B=10 Mb/s

Fig. 5.8 (b)

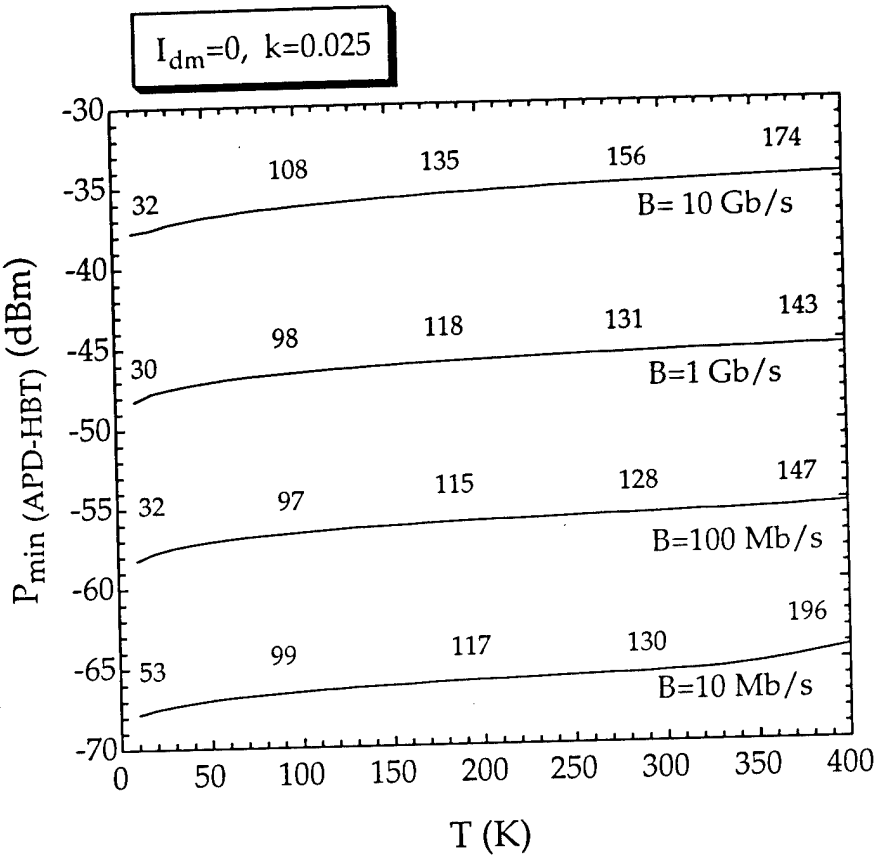
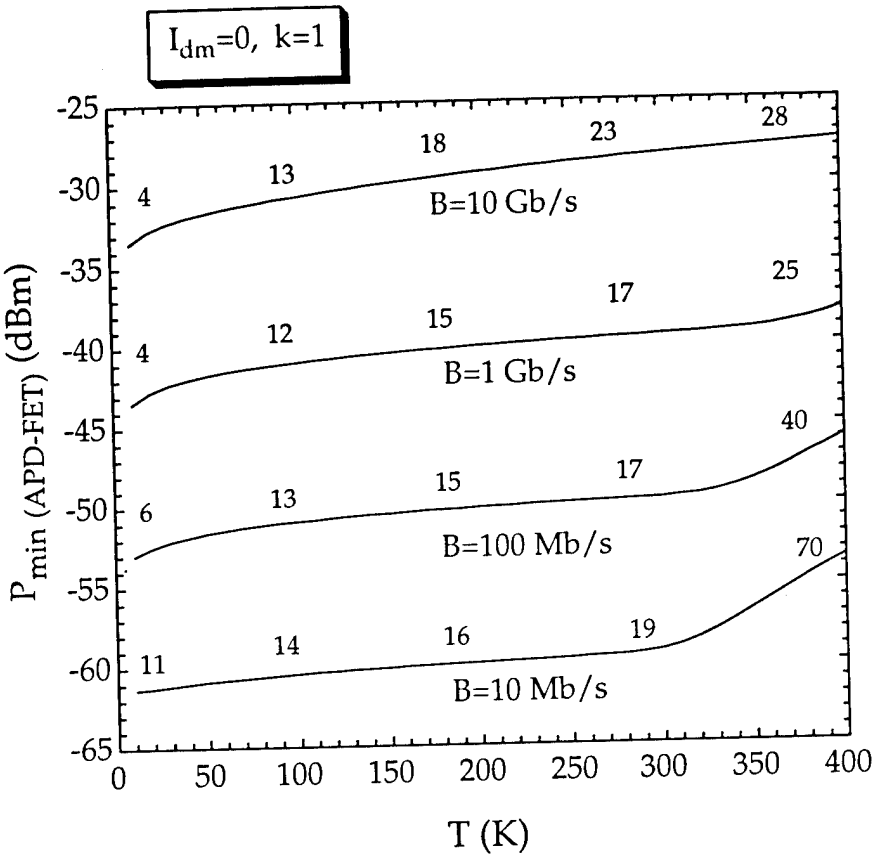

I_{dm}=0, k=0.025
P_{min} (APD-HBT) (dBm)
-30
-35
-40
-45
-50
-55
-60
-65
-70
0
50
100
150
200
250
300
350
400
T (K)
32
108
135
156
174
B= 10 Gb/s
30
98
118
131
143
B=1 Gb/s
32
97
115
128
147
B=100 Mb/s
53
99
117
130
196
B=10 Mb/s

Fig. 5.8 (c)



(a)

Fig. 5.9: Receiver sensitivity as a function of temperature for different values of bandwidth for an APD/FET receiver for I_{dm}=0 and (a) k=1, (b) k=0.5, and (c) k=0.025. The values for the avalanche gain that minimizes the required power, M_{opt}, are given next to each line.

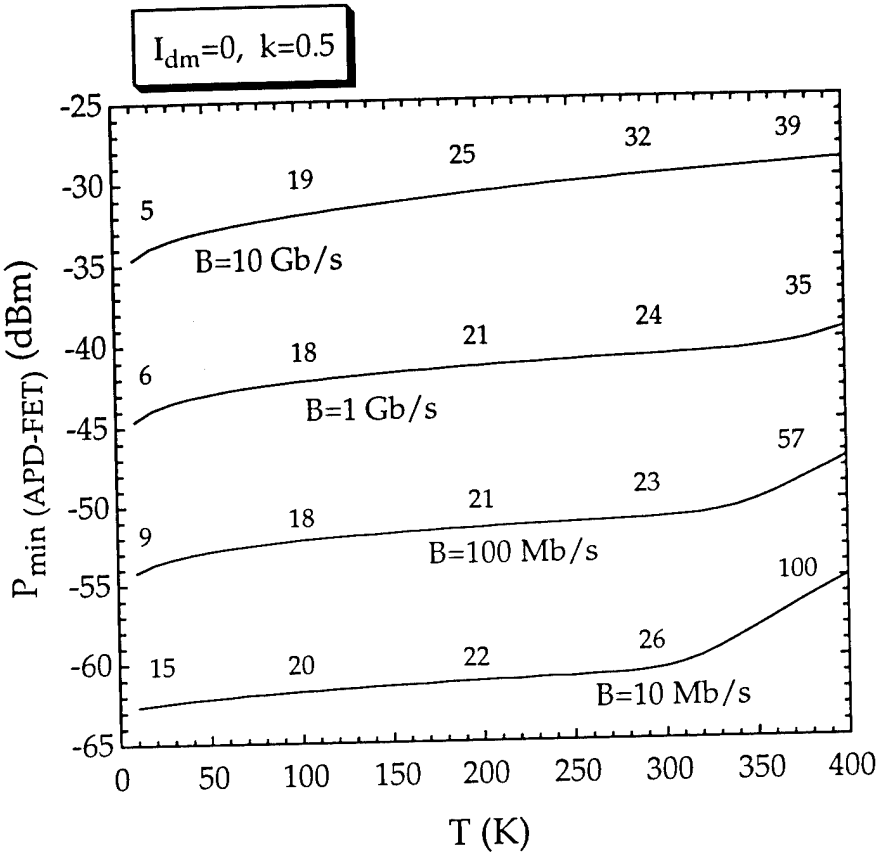

I_{dm}=0, k=0.5
-25
-30
-35
-40
-45
-50
-55
-60
-65
P_{min} (APD-FET) (dBm)
0
50
100
150
200
250
300
350
400
T (K)
5
19
25
32
39
B=10 Gb/s
6
18
21
24
35
B=1 Gb/s
9
18
21
23
57
B=100 Mb/s
15
20
22
26
100
B=10 Mb/s

Fig. 5.9 (b)

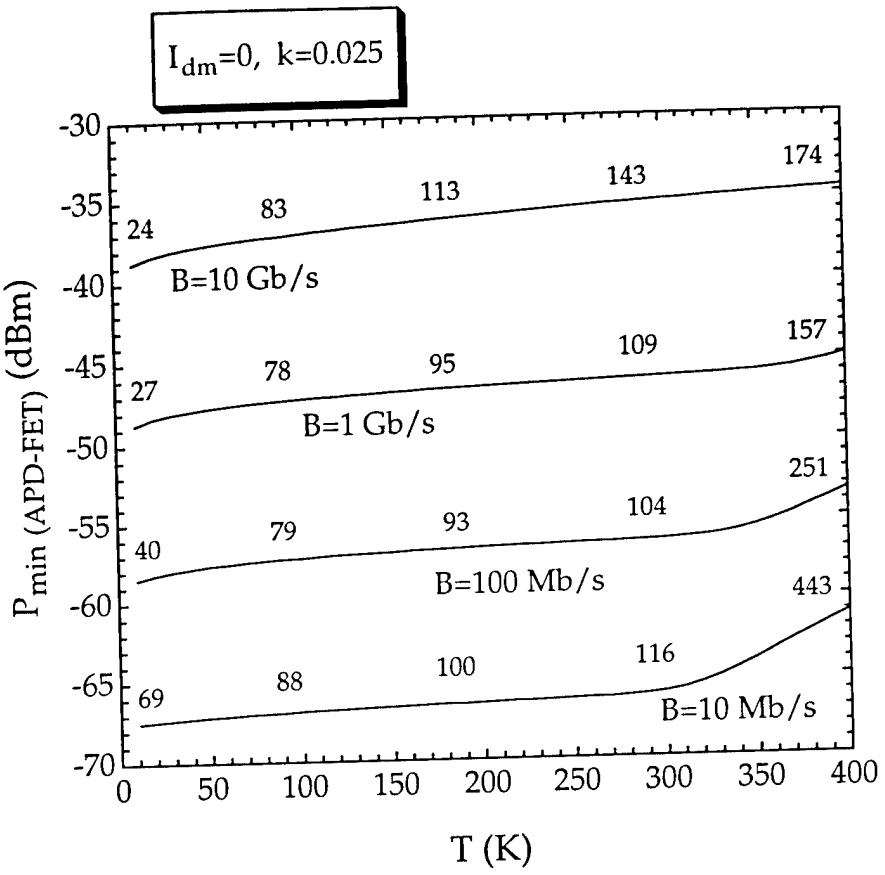

I_{dm}=0, k=0.025
-30
-35
-40
-45
-50
-55
-60
-65
-70
P_{min} (APD-FET) (dBm)
24
83
113
143
174
B=10 Gb/s
27
78
95
109
157
B=1 Gb/s
40
79
93
104
251
B=100 Mb/s
69
88
100
116
443
B=10 Mb/s
0
50
100
150
200
250
300
350
400
T (K)

Fig. 5.9 (c)

improves by ~1.5 dB when k is reduced from 1 to 0.5, and then by another 5 dB as k is further reduced to 0.025, or a total improvement of 6.5 dB. Here, similarly to the p-i-n-based receivers, the temperature dependence is weak, resulting in only about a 2 dB improvement for T=400 K down to 77K for the APD/HBT. For APD/FET case, despite the strong T-dependence between 400K and 300K, there is only a 2 dB improvement below 300K.

It can also be seen that for a given value of k, the value of M_{opt} (avalanche gain which minimizes P_{min}) increases at higher temperatures to compensate for the increased noise currents (see Eq. 5.20). In addition, as k gets smaller, the value of M_{opt} increases. The reason can be seen in Eq. 5.22, which indicates smaller dependence of excess noise factor (F) on M for lower k values. Higher values of avalanche gain can be obtained by increasing the applied voltage to the device. While the breakdown voltage (i.e. the voltage at which the multiplication becomes infinite) increases at higher temperatures[8], thus facilitating the required increase of M_{opt} for these regimes, the maximum value of M_{opt} may be limited by this voltage.

It is important to note that α and β are both inversely proportional to the mean free path of the corresponding carrier, λ_e or λ_h. As λ increases with decreasing temperature, it is expected that the ionization coefficients, α and β would subsequently decrease[25]. The change in the value of k with temperature is dependent on the relative changes of α and β, which is governed by the ionization threshold energies of electrons and holes. Fig. 5.10 shows the change in k as a function of temperature for different materials. In this analysis, we have assumed constant values for k.

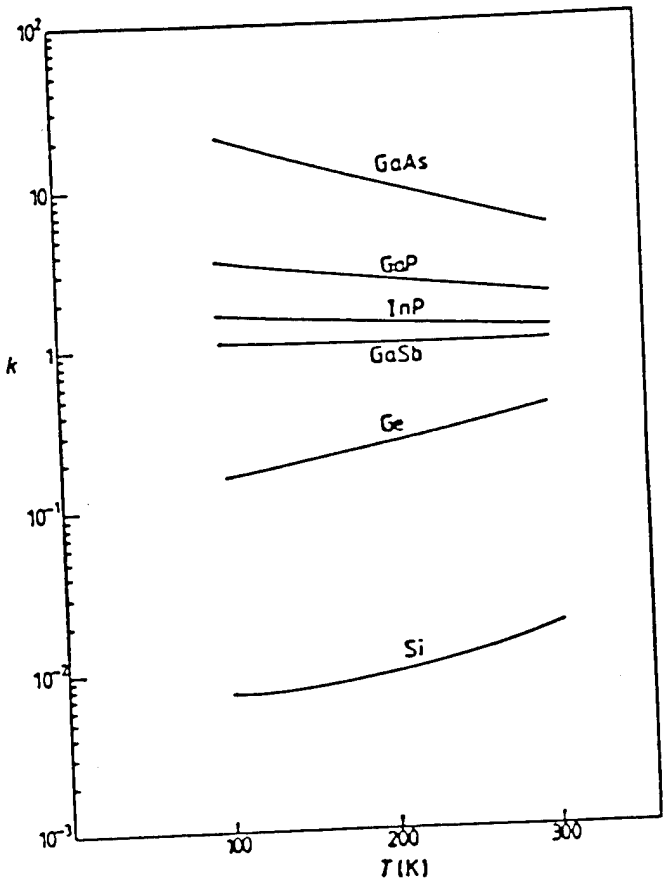


Fig. 5.10: Temperature dependence of k at x_h=12.5 ($x_h=E_i/eE\lambda_h$ where E_i is the ionization threshold energy, e is the electron charge, E is the electric field, and λ_h is the hole mean free path[9]).

5.3.2 APD based receivers with $I_{dm}>0$

As mentioned earlier, the dark current in the APD may be largely due to bulk processes, in which case, it will undergo the avalanche process. The result will be an increase in the shot noise of the detector[4]:

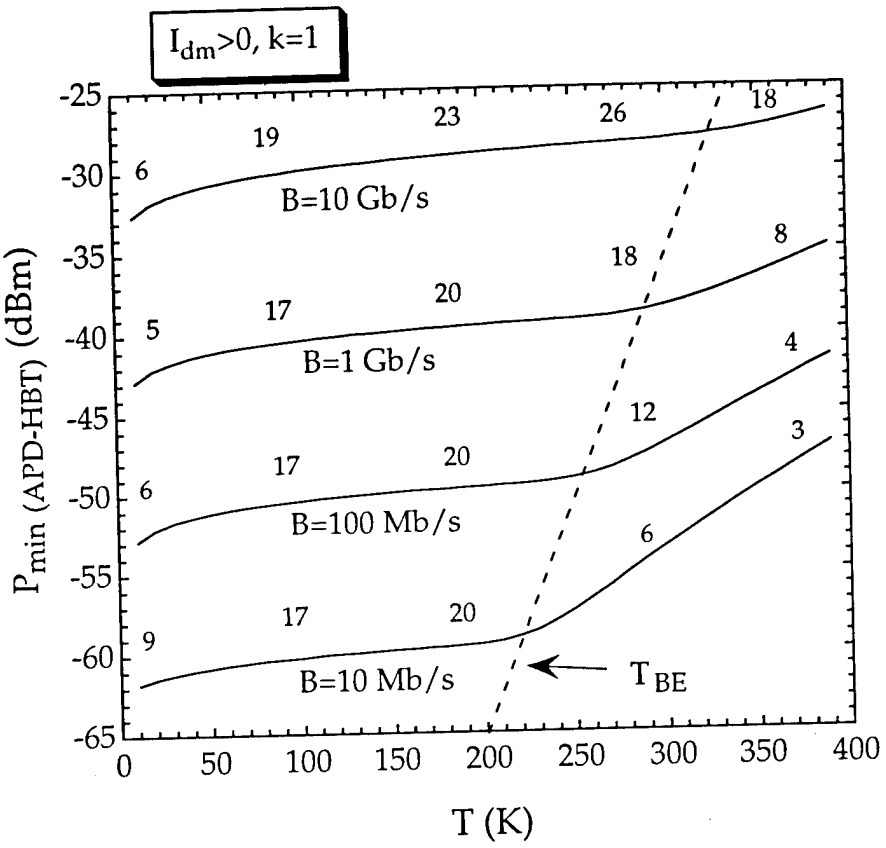
$$< i_t^2 >_{APD} = 2q(I_{du} + M^2F(M)I_{dm})I_2B \tag{5.23}$$

where all the unmultiplied dark current from the APD and the amplifier have been included in a single term I_{du}, and the primary dark current that undergoes multiplication is equal to I_{dm}. In order to keep with the same convention of expressing P_{APD} in terms on P_{pin}, the multiplied dark current contribution to the shot noise can be added to Eq. 5.20 to result[4]:

$$\eta P_{min(APD)} = [(\frac{\eta P_{min(pin)}}{M})^2 + 2q(\frac{hc}{q\lambda})^2 Q^2 F(M) I_2 B]^{1/2} + (\frac{hc}{\lambda}) Q^2 F(M) I_1 B. \tag{5.24}$$

Similarly to the previous case, we have substituted expression for the p-i-n/HBT and p-i-n/FET cases and evaluated the P_{min} for the schemes where an APD with multiplied dark current is used as the detector. The calculations are performed for k=1, 0.5, and 0.025. Results are plotted in Fig. 5.11 (a), (b), (c) for APD/HBT and in Fig. 5.12 (a), (b), (c) for APD/FET.

The following observation can be made from the simulation results: In APD/HBT and APD/FET cases, although M_{opt} increases at lower k values, the rate of this increase and the magnitude of M_{opt} are much smaller than in the corresponding $I_{dm}=0$ case. The reason is that while M_{opt} can be higher for lower k due to lower excess noise, it increases shot noise through multiplication of I_{dm} by M_{opt}^2, and hence the value of M_{opt} reflects this



(a)

Fig. 5.11: Receiver sensitivity as a function of temperature for different values of bandwidth for an APD/HBT receiver for I_{dm}>0 and (a) k=1, (b) k=0.5, and (c) k=0.025. The values for the avalanche gain that minimizes the required power, M_{opt}, are given next to each line. The dashed line indicates the break even temperature, T_{BE}, below which multiplication of dark current (I_{dm}) has no effect.

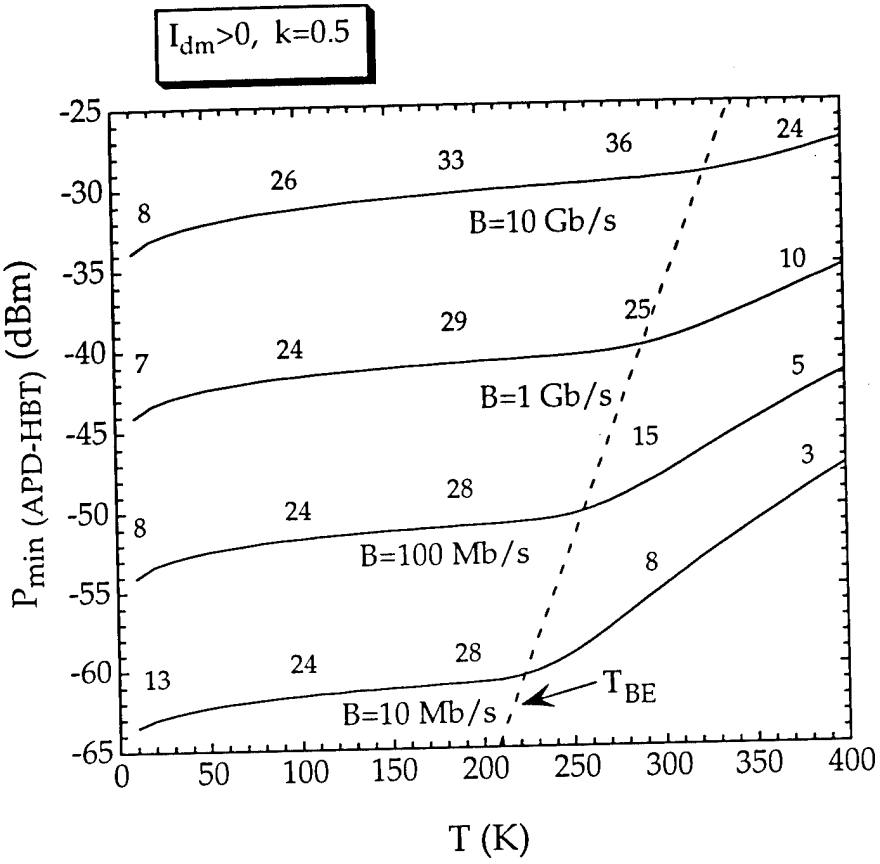

I_{dm}>0, k=0.5
-25
-30
-35
-40
-45
-50
-55
-60
-65
0
50
100
150
200
250
300
350
400
P_{min} (APD-HBT) (dBm)
T (K)
B=10 Gb/s
B=1 Gb/s
B=100 Mb/s
B=10 Mb/s
T_{BE}
8
26
33
36
24
7
24
29
25
10
8
24
28
15
5
13
24
28
8
3

Fig. 5.11 (b)

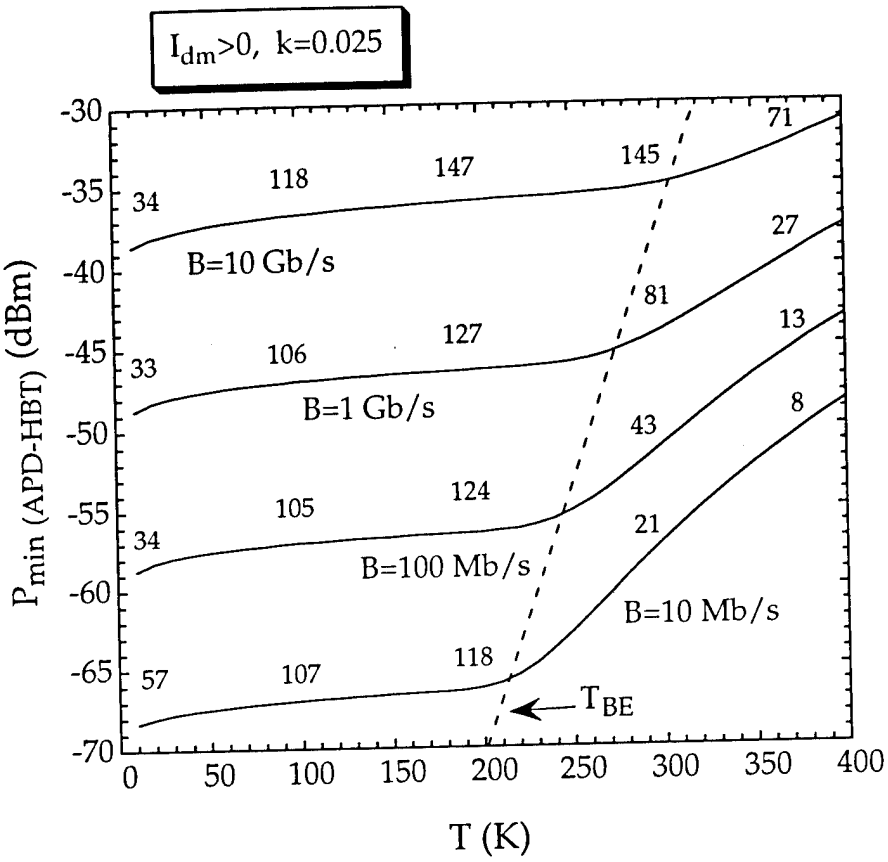
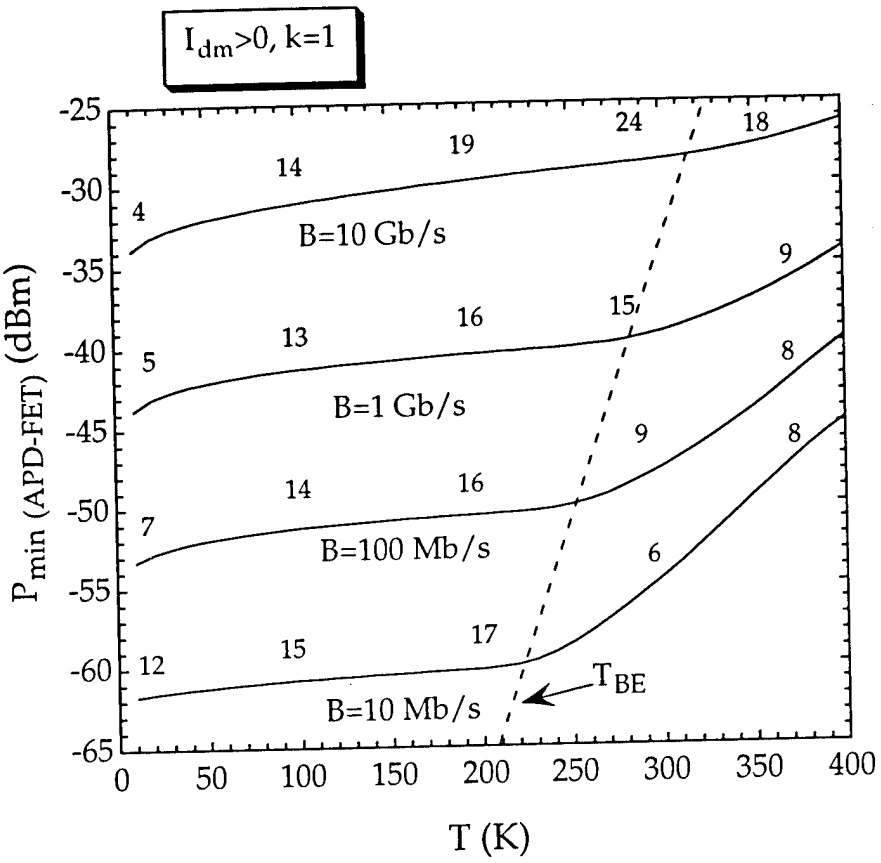

I_{dm}>0, k=0.025
P_{min} (APD-HBT) (dBm)
T (K)
B=10 Gb/s
B=1 Gb/s
B=100 Mb/s
B=10 Mb/s
T_{BE}
-30
-35
-40
-45
-50
-55
-60
-65
-70
0
50
100
150
200
250
300
350
400
34
118
147
145
71
33
106
127
81
27
34
105
124
43
13
57
107
118
21
8

Fig. 5.11 (c)



(a)

Fig. 5.12: Receiver sensitivity as a function of temperature for different values of bandwidth for an APD/FET receiver for $I_{dm}>0$ and (a) k=1, (b) k=0.5, and (c) k=0.025. The values for the avalanche gain that minimizes the required power, M_{opt}, are given next to each line. The dashed line indicates the break even temperature, T_{BE}, below which multiplication of dark current (I_{dm}) has no effect.

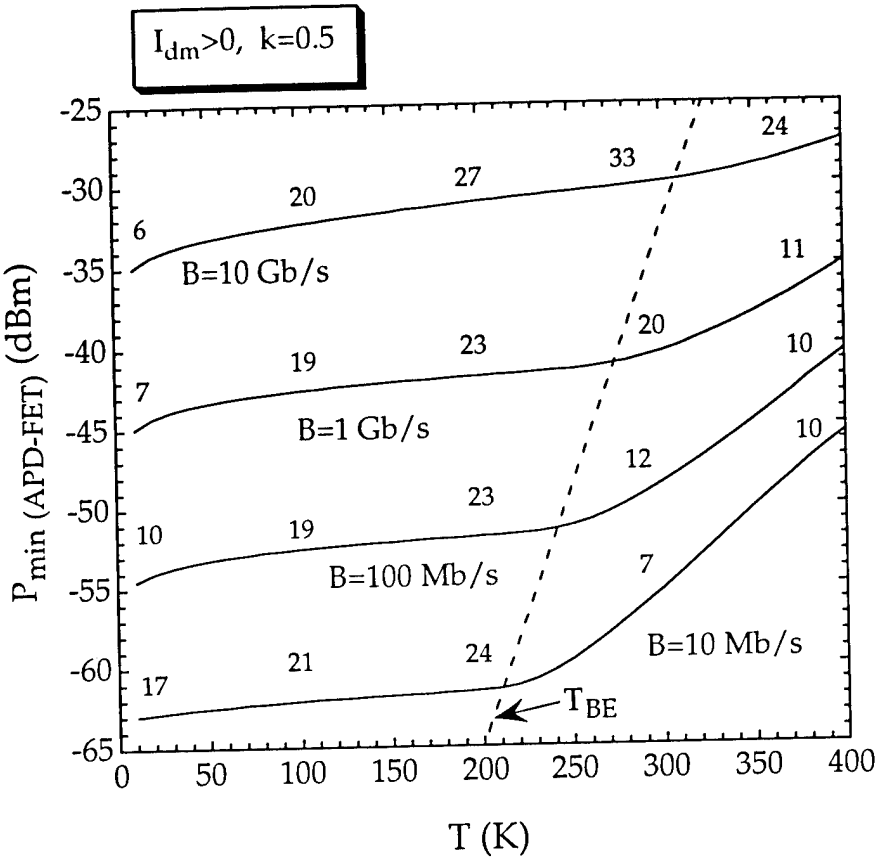

I_{dm}>0, k=0.5
-25
-30
-35
-40
-45
-50
-55
-60
-65
P_{min} (APD-FET) (dBm)
0
50
100
150
200
250
300
350
400
T (K)
B=10 Gb/s
B=1 Gb/s
B=100 Mb/s
B=10 Mb/s
T_{BE}
6
20
27
33
24
7
19
23
20
11
10
10
19
23
12
10
17
21
24
7

Fig. 5.12 (b)

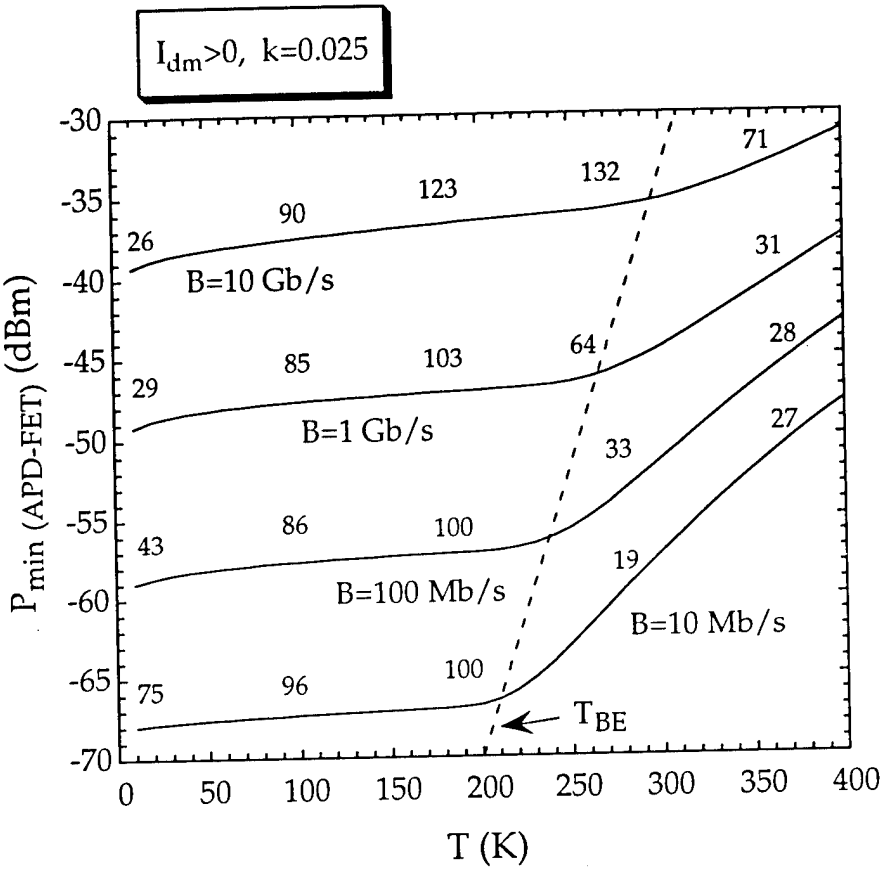

I_{dm}>0, k=0.025
P_{min} (APD-FET) (dBm)
T (K)
B=10 Gb/s
B=1 Gb/s
B=100 Mb/s
B=10 Mb/s
T_{BE}
-30
-35
-40
-45
-50
-55
-60
-65
-70
0
50
100
150
200
250
300
350
400
26
90
123
132
71
29
85
103
64
31
43
86
100
33
28
75
96
100
19
27

Fig. 5.12 (c)

tradeoff. That is also why in $I_{dm}>0$ case, M_{opt} decreases for regions where the effect of I_{dm} is most prominent (i.e. low bandwidth, and high temperatures).

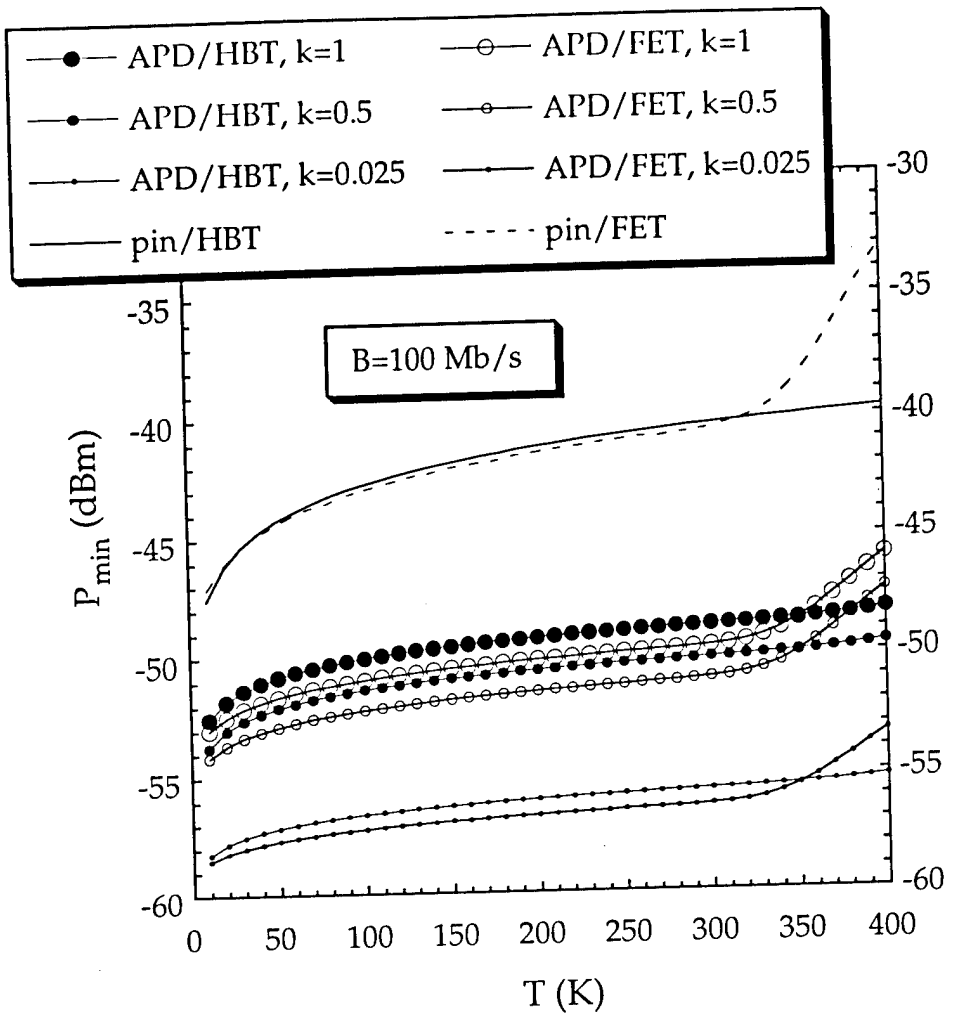
In order to further study the effects of $I_{dm}>0$ we define the break even temperature, T_{BE}, as the temperature where P_{min} for $I_{dm}>0$ and $I_{dm}=0$ cases are identical. It can be seen in the Fig. 5.11 and 5.12 that $T_{BE}\approx 200K$ at B=10 Mb/s for both receiver types, but it increases at higher bandwidth, as the relative importance of shot noise (which includes I_{dm}) decreases for these regions. Clearly, for $I_{dm}>0$ cases, operation temperature needs to be less than T_{BE} to avoid the sharp sensitivity degradation.

5.4 Comparison of different approaches

5.4.1 Relative sensitivity

Cumulative plots of the minimum required power at B=100 Mb/s and 1 Gb/s for different detection and amplification schemes studied here are given in Fig. 5.13 (a), (b). The $I_{dm}>0$ cases have not been included as they are only useful for $T<T_{BE}$, where their performance is identical to $I_{dm}=0$ cases. For both bandwidths, the lowest required power is obtained using an APD/FET. For this case, at B=100 Mb/s, P_{min}=-56 dBm to -58 dBm as temperature changes from room temperature to 77 K. This sensitivity degrades at B=1 Gb/s such that P_{min}=-46 dBm at T=300 K, and improves to P_{min}=-48 dBm for T=77 K.

As seen in this figure, for HBT-based amplifiers at T=300 K, there is an 8 dB advantage in using APD's instead of p-i-n photodiodes. For FET based receivers, this advantage is about 9 dB. This advantage decreases at low temperatures, since M_{opt} gets smaller for this regime.



(a)

Fig. 5.13: Receiver sensitivity as a function of temperature for (a) B=100 Mb/s and (b) B=1 Gb/s.

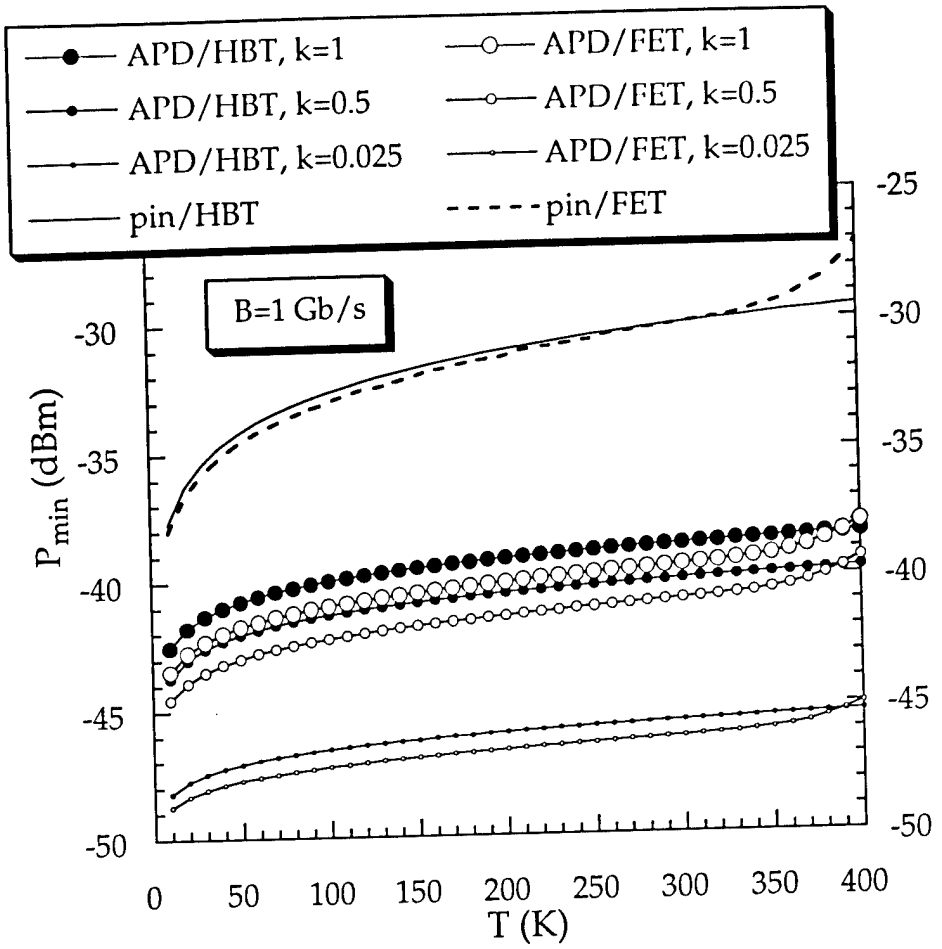

APD/HBT, k=1
APD/HBT, k=0.5
APD/HBT, k=0.025
pin/HBT
APD/FET, k=1
APD/FET, k=0.5
APD/FET, k=0.025
pin/FET
B=1 Gb/s
P_{min} (dBm)
-30
-35
-40
-45
-50
-25
-30
-35
-40
-45
-50
0
50
100
150
200
250
300
350
400
T (K)

Fig. 5.13 (b)

We have also plotted switching energies (E_{sw}) for various detection and amplification schemes @B=100 Mb/s and B=1 Gb/s in Fig. 5.14 (a), (b). It was mentioned earlier that $E_{sw}=P_{min}/\Delta f$ where $\Delta f \sim I_2 B$ for an NRZ coding scheme. As expected, the values of E_{sw} follow the same pattern as the sensitivity values for given bit rates. For T<300 K, the switching energies are independent of bit rate for both cases. This is due to the dominance of Johnson noise (see Eq. 5.2) where $\langle i_r^2 \rangle \sim B^2$, thus $P_{min} \sim B$ (from Eq. 5.11), and hence the frequency dependence cancels out. For T>300 K, shot noise dominates and $\langle i_t^2 \rangle \sim B$, thus $E_{sw} \sim B^{-1/2}$. Therefore, for this temperature range E_{sw} for B=100 Mb/s is larger than the case when B=1 Gb/s.

5.4.2 Discussion on practicality of each approach

Although it has been shown in the discussion above that APD/FET combination provides the highest sensitivity, there are practical problems that prohibit a wide range use of this receiver type. The APD performance is strongly related to the material quality, and the growth of a supperlattice structure to provide a lower k is far more difficult than that of a p-i-n. Furthermore, APD operating voltages may be as high as 100 V, which is much higher than the required circuit bias supply (about 3 V) and maybe impractical. In addition, the temperature dependence of breakdown voltage may limit the achievable values of M_{opt} at low temperatures. Therefore, for many applications, p-i-n's are more suitable.

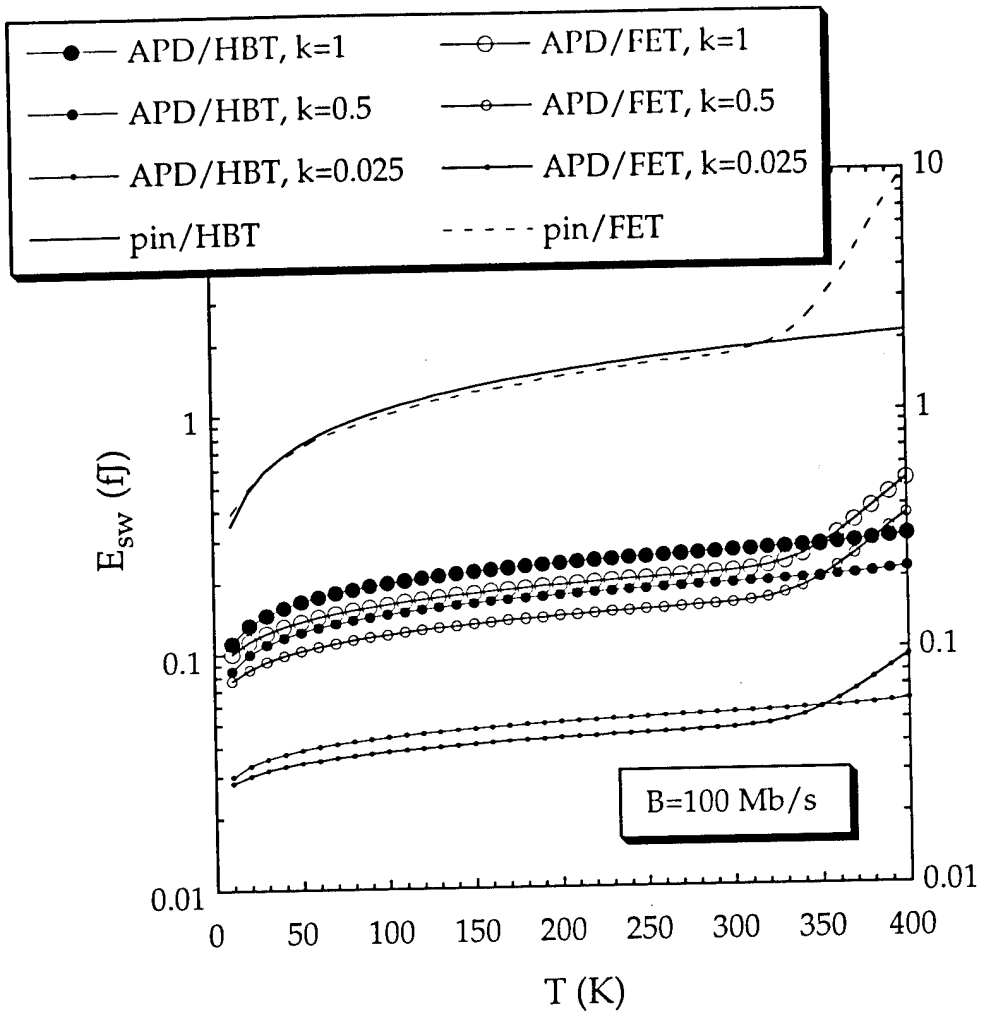


Fig. 5.14: Receiver switching energy as a function of temperature for (a) B=100 Mb/s and (b) B=1 Gb/s.

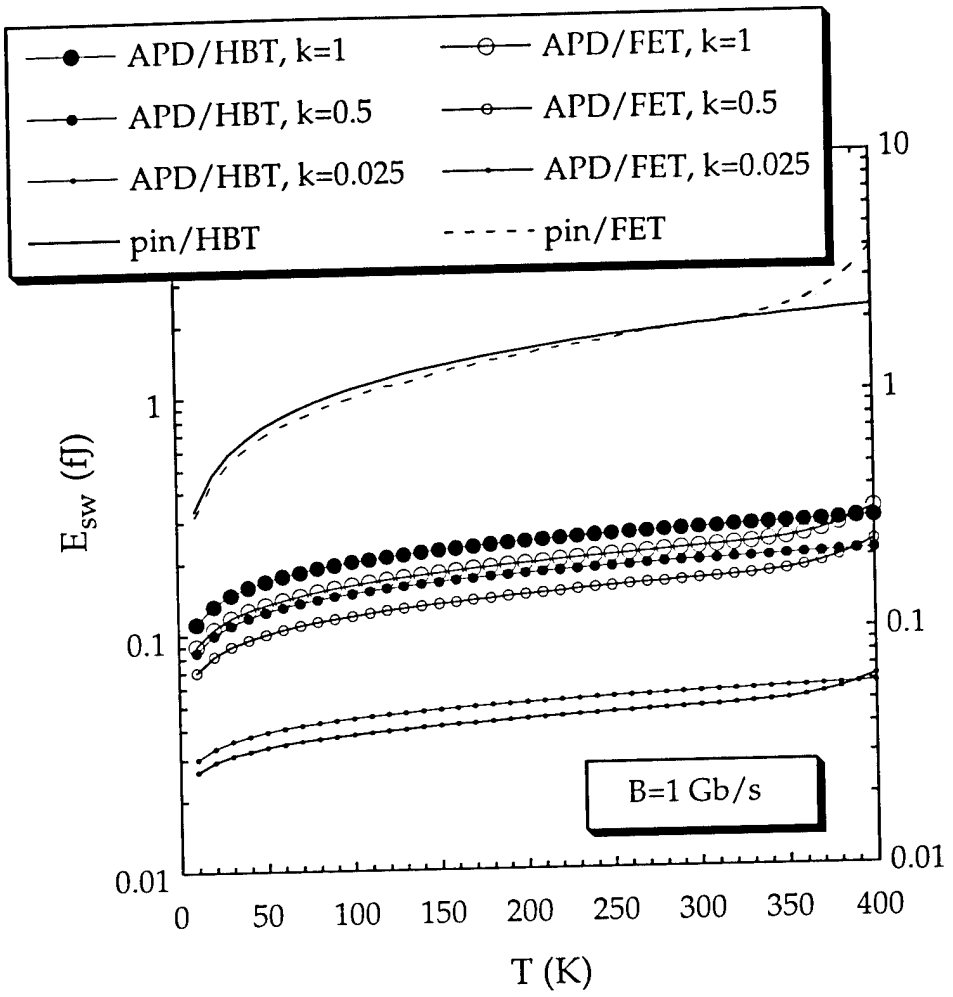

APD/HBT, k=1
APD/HBT, k=0.5
APD/HBT, k=0.025
pin/HBT
APD/FET, k=1
APD/FET, k=0.5
APD/FET, k=0.025
pin/FET
B=1 Gb/s
E_{sw} (fJ)
T (K)
10
1
0.1
0.01
0
50
100
150
200
250
300
350
400

Fig. 5.14 (b)

5.5 RIN-noise

High sensitivity receiver/transmitter circuits are able to detect and amplify very low power signals. An important issue in the transmission of such low level signals is the relative intensity noise (RIN) in the output laser[26]. The optical power emitted by a semiconductor laser is not constant, and it fluctuates around its steady state value. RIN is a parameter used to characterize this fluctuation, and for a given frequency ω it is defined as:

$$RIN = S_p(\omega)/P^2 \tag{5.25}$$

where $S_p(\omega)$ is the spectral density and P is the steady state emitted power.

At a given power level, noise is relatively low when $\omega << \Omega_R$, and it is enhanced significantly when in the vicinity of $\omega = \Omega_R$, where Ω_R is the relaxation-oscillation frequency. For different frequency regimes, the dependence of RIN on power given in Eq. 5.25 varies depending on the power level. When $\omega << \Omega_R$, RIN dependence on P is as P^{-3} for low power levels and as P^{-1} for higher powers. Therefore, RIN not only introduces a limitation in the power, but also in the operation frequency.

The effect of high RIN at power levels near the sensitivity limit can be reduced by designing a large gain circuit, such that the output optical power is high. Furthermore, the bit rate should be chosen such that it is sufficiently away from Ω_R. The design goal, then, should be a high sensitivity front end followed by high gain amplification stages, and an optimized bandwidth.

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Chapter 6

Conclusions and Future Work

6.1 Conclusions

We have demonstrated an ultra low switching energy optoelectronic smart pixel fabricated in the InP/InGaAsP materials system. The smart pixel studied in this work has a switching energy of 14 fJ when taken as a stand-alone receiver. With gain and cascadability, the switching energy is 30 fJ. These are the lowest values of switching energy obtained to date for smart pixel technologies[1-4]. These low switching energies were obtained while also optimizing the other figures of merit for the pixel, i.e. gain, bandwidth, and power dissipation. These factors arise from system requirements for potential applications of smart pixel arrays discussed in Ch. 1.

This pixel utilizes a hybrid/integrated component assembly, i.e. while all the receiver components are monolithically integrated, the output device (a folded cavity surface emitting laser, FCSEL) is surface bonded onto the pixel. The smart pixel wafer was grown using gas source molecular beam epitaxy (GSMBE). The strained InGaAsP multiple quantum well (MQW) FCSEL used as the output device has a threshold current of 24 mA. This is the lowest value of threshold current obtained to date for such devices fabricated in the InP materials system. This work, therefore, represents an

advancement in material growth, design and fabrication of long wavelength OEIC's.

The optoelectronic circuit has optical input and output with electronic processing, and operates at 1.3 μm wavelength, hence making it compatible for use at the interface of long wavelength fiber-optic networks and board-level optoelectronic interconnections. The circuit has amplification (I/O optoelectronic gain=8), the ability to drive subsequent gates (fan-out=3), the ability to be cascaded in a multi-stage system (cascadability), and switching capability (both linear and thresholding). These functions constitute the "intelligence" of the pixel. The bandwidth of the smart pixel was 100 Mb/s for an NRZ data format. The circuit can be enabled/disabled via electrical control.

We have performed theoretical calculations based on noise analysis techniques to compare sensitivity of several different detection schemes as a function of bandwidth and temperature. These schemes include APD or p-i-n photodetectors in conjunction with HBT or FET-based amplifiers. The analyses show that the best sensitivity is achieved with an APD/FET receiver. The sensitivity has been shown to depend on bit rate and temperature, with an improvement in sensitivity predicted as temperature is reduced. Sensitivity degrades at higher bit rates, although its improvement at lower temperatures at high bit rates becomes more significant.

In conclusion, we have addressed issues regarding the use of long-wavelength smart pixel technology for optoelectronic interconnections, focusing largely on switching energy, integration, and power dissipation issues. The pixel demonstrated here has the lowest switching energy for comparable devices studied to date. Based on noise analysis, we have then

calculated the optimum limits for sensitivity (and thus switching energy), and found detection schemes with performances considerably higher than those currently under consideration.

6.2 Future Work

The design of the smart pixel circuit presented here was the first generation of such circuits, and lays the groundwork for future monolithically integrated pixels with improved performance. The low switching energy of the device is largely due to the inclusion of the feedback resistor and the performance of circuit HBT's. However, with the current circuit configuration, the bandwidth also degrades as a result of this feedback. The pixel bandwidth can be readily improved by including a multi-stage front end where the effect of the feedback is distributed over several stages, or via a cascode configuration. To improve the bandwidth and hence the switching energy of the pixel, collector-base junction capacitance also needs to be reduced. This can be accomplished by reducing the area of the HBT's, and lowering the background doping in the collector.

The circuit diagram for a proposed second generation smart pixel circuit is shown in Fig. 6.1 (courtesy of D. S. Kim). This pixel uses a monolithically integrated FCSEL which is to be fabricated on the same substrate by addition of a few layers to the epitaxial structure, and modifying the photolithography mask layers. The added features will improve the bandwidth (predicted to be 800 MHz), sensitivity and thus switching energy of the pixel. In addition, the surface bonding and associated reactances will be eliminated. On the other hand, the complexity of the circuit, material growth, and fabrication will increase.

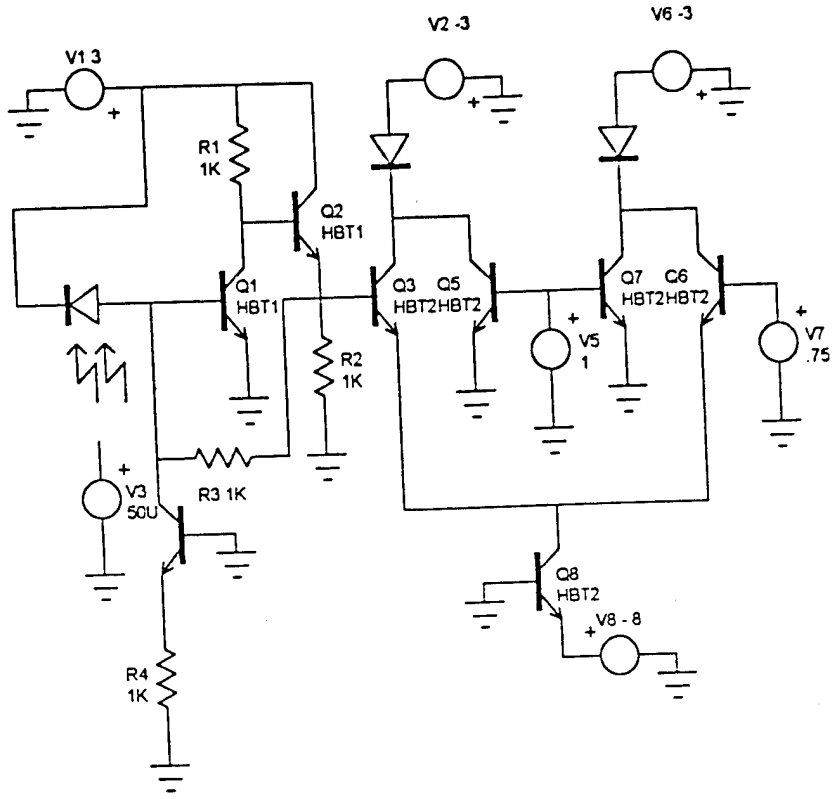

Fig. 6.1: Circuit diagram for a second generation monolithically integrated smart pixel.

Potential applications for the smart pixels include crossbar switching networks and spatial light modulators (SLM's). The functionality of the pixel in such systems enhances the overall system performance. In both of these systems, two dimensional arrays of smart pixels are required. Thus, fabrication of smart pixel arrays (2x2 and larger) is the next step, after optimizing individual pixel performance. With these arrays, an imaging system must be employed in order to perform routing of the input/output optical beams. The imaging system can use index-guided optical interconnections (using fibers or optical waveguides integrated on the substrate), or free-space optical interconnections (using lenses or holograms)[5]. The assembly will then need to be packaged using flip-chip or wire bonding for mechanical robustness, ease of characterization and system implementation.

References

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Appendix A

Derivations of the circuit equations

A.1 The effect of signal current on base and feed back currents

From the small signal model of the front end (Fig. 2.7), and writing two node equations and one voltage loop equation, it can be seen that the ratio of the signal flowing through the feedback resistor R_f, to the signal current through the base can be written as:

$$\frac{I_{fs}}{I_{bs}} = \frac{r_{bb}+r_\pi+g_m r_\pi R_c}{R_f+R_c} \approx \frac{\beta(1+g_m R_c)/g_m}{R_f+R_c} \approx \frac{\beta R_c}{R_f+R_c} = 44 \qquad (1)$$

where we have assumed that $r_{bb}+r_\pi \approx r_\pi$, and $g_m R_c >> 1$.

Therefore, the factor D_{bs} defined as the ratio of the signal induced base current to the total signal current can be written as:

$$D_{bs} = \frac{I_{bs}}{I_{ph}} = \frac{1}{1+\frac{\beta R_c}{R_f+R_c}} \approx \frac{R_f+R_c}{\beta R_c} = 0.02 \qquad (2)$$

A.2 Front end Voltage Swing

It is apparent that:

$$\begin{aligned} \beta I_{b_1} &= I_{c_1} \\ I_{b_1} &= I_{Ph} - I_f \\ I_f &= \frac{V_b - V_c}{R_f} \end{aligned} \qquad (3)$$

hence, $\beta(I_{Ph} - \frac{V_b - V_c}{R_f}) = I_c$ (4)

also,

$$I_c = \frac{V_{cc} - V_c}{R_c} + \frac{V_b - V_c}{R_f} - I_{b_2} \quad (5)$$

where I_{b2} is the base current of Q_2.

Combine (4), (5):

$$I_{Ph} = \frac{R_f V_{cc} - V_c(R_f + R_c + \beta R_c) + V_{b1}(R_c + \beta R_c) - I_{b2} R_1 R_2}{\beta R_c R_f} \quad (6)$$

Thus:

$$\Delta I_{Ph} = \frac{-\Delta Vc(R_f + R_c + \beta R_c)}{\beta R_c R_f} + \frac{\Delta V_{b1}(R_c + \beta R_c)}{\beta R_c R_f} - \frac{\Delta I_{b2}}{\beta} \quad (7).$$

Therefore,

$$\Delta I_{ph} = \frac{-\Delta V_c}{R_f} + \frac{\Delta V_{b1}}{R_f} \quad (8)$$

and

$$\Delta V_c = -R_f \Delta I_{ph} \quad (9)$$

using this value, the change in the base voltage of Q_1 can be found to be:

$$\Delta V_b = R_f I_{b_1} \quad (10).$$

The change in I_C can be calculated from above equations to be:

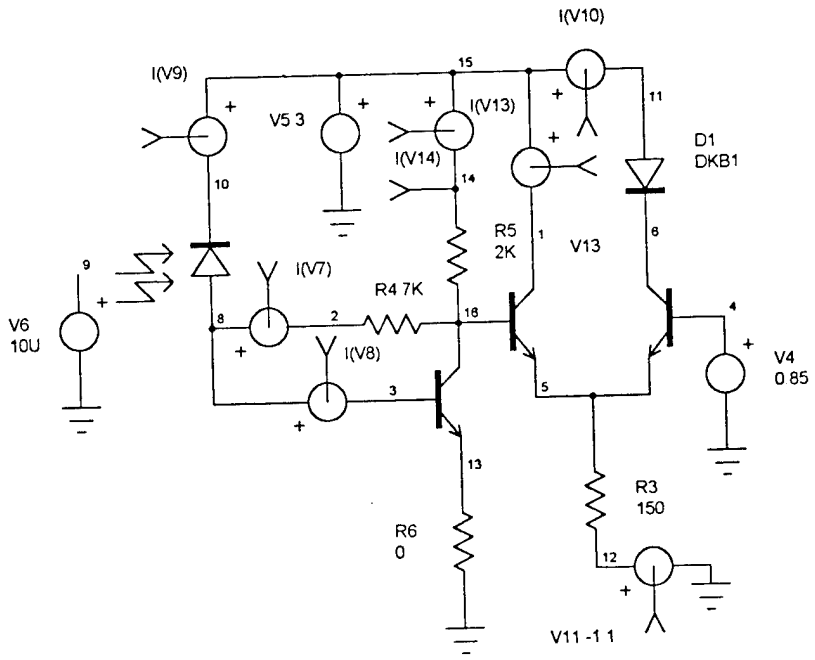
$$\Delta I_c = \Delta I_{ph}(\frac{R_f}{R_c} + 1) \quad (11)$$

The base current of Q1 changes by less than 1 uA, and hence the change in the base voltage of Q1 is very small. Therefore, the 2nd and the 3rd terms can be ignored.

Appendix B

Details of the SPICE Simulation for the Smart Pixel Circuit

B.1: The smart pixel circuit diagram in SPICE



B.2: The SPICE text file for the smart pixel circuit

```
C:\SPICE4\USERSP\KIAN\KBSLM
*SPICE_NET
*INCLUDE OCMLIB\KB1.LIB
.DC V6 0 100U 0.1U
*.AC DEC 100 100K 1G
.PRINT DC I(V10) V(16)
.PRINT AC  I(V10) IP(V10)
Q3 6 4 5 KNBJT
V4 4 0 0.85
R3 5 12 150
D1 11 6 DKB1
Q4 16 3 13 KNBJT
R4 2 16 7K
R5 14 16 2K
V5 15 0 3
X1 9 10 8 PINPD
V6 9 0 10U AC 5U
V7 8 2 0
V8 8 3
V9 15 10
V10 15 11
V11 12 0 -1.1
V13 15 1
V14 15 14
R6 13 0 0
Q2 1 16 5 KNBJT
.END
```

B.3: The library of component values for the SPICE simulation

```
**********************************NPN HBT
.MODEL KNBJT NPN(CJC=300fF TF=1E-12 BF=200 TR=1E-12 VJE=.8 RE=100
+ CJE=400fF  RC=100 RB=1K VAF=7 IKF=15E-3 IS=1E-13 VJC=.6 NF=1.2
+ NE=1.5)
**********************************
.MODEL Dkb1 D (IS=2N RS=10 N=1 BV=15 IBV=2U
+ CJO=340E-15 VJ=0.714 M=.5 EG=0.76)
**********************************
****************SPICE PARAMETER FOR InGaAs PHOTORECEIVER*********
.MODEL JSY1 NJF (VTO=-1.5 BETA=8.76E-03 LAMBDA=.02
+ RD=17 RS=200 IS=3E-11
+ PB=0.714 FC=.5 CGS=100E-15 CGD=17E-15)
* InGaAs DEPLETION  N-Channel
****************************************
*SYM=BPW34
.SUBCKT PINPD  4               1         3
*              Input Pwr(W)    Cathode   Anode
D2 6 1 DSY1
G2 1 6 POLY(2) 1 6 4 0 0 2N 0.8
* Dark current
V4 6 3 ;  Photodiode Current
.MODEL DSY1 D (IS=2N RS=10 N=1 BV=15 IBV=2U
+ CJO=800e-15 VJ=0.714 M=.5 EG=0.75)
*Photodiode model made by SpiceMod
.ENDS
****************
```

Appendix C

Process Sheets for Smart Pixel Fabrication

Emitter Mesa Etch

Wafer Number	PB 110294
Date	12/14/94

Process	Parameters			Remarks
Preparation	Tergitol 10:1 + DI water clean			
	30 min prebake at 115° C			Oven
	Iso-Propanol rinse while spinning			
Photolith	Photoresist		4110 AZ	
	Speed		4 krpm	
	Time		40 sec	
	Prebake	Temp	100 °C	Hot Plate
		Time	2 min	
	Exposure	Power	275 W	
		time	3.0 sec	
	Developer	400 K		
		Conc.	4:1	
		Time	55 sec	
	De-Scum method		O_2 Plasma	
	RIE Machine		μ-RIE	
	Pressure		300 mtorr	
	Power		100 W	
	Time		1 min	
	Postbake	Temp	115 °C	Oven
		Time	30 min	
Etching	Chemical	Ratio		
	50% Citric:H_2O: H_2O_2	5:5:1		
	Material	InGaAs		
	Time	3 min		
	Total Etch Depth	0.2 μm		
Etching	Chemical	Quantity		
	$HCl:H_3PO_4:H_2O$	3:1:3		
	Material	InP		
	Time	2 min		
	Total Etch Depth	0.4 μm		undercut
PR Strip	Solvent	Acetone +Iso		
	De-scum Machine	μ-RIE		same as above
		Time	4 min	

Base-Collector Mesa Etch

Wafer Number	PB 110294
Date	12/15/94

Process	Parameters			Remarks
Preparation	Tergitol 10:1 + DI water clean			
	30 min prebake at 115° C			Oven
	Iso-Propanol rinse while spinning			
Photolith	Photoresist		4110 AZ	
	Speed		4 krpm	
	Time		40 sec	
	Prebake	Temp	100 °C	Hot Plate
		Time	2 min	
	Exposure	Power	275 W	
		time	3.0 sec	
	Developer	400 K		
		Conc.	4:1	
		Time	55 sec	
	De-Scum method		O_2 Plasma	
	RIE Machine		μ-RIE	
	Pressure		300 mtorr	
	Power		100 W	
	Time		1 min	
	Postbake	Temp	115 °C	Oven
		Time	30 min	
Etching	Chemical	Ratio		
	50% Citric:H_2O: H_2O_2	5:5:1		
	Material	InGaAs		
	Time	3 min		
	Total Etch Depth	0.38 μm		
Etching	Chemical	Quantity		
	$HCl:H_3PO_4:H_2O$	3:1:3		
	Material	InP		
	Time	40 sec		
	Total Etch Depth	0.43 μm		undercut
PR Strip	Solvent	Acetone +Iso		
	De-scum Machine	μ-RIE		same as above
		Time	4 min	

Sub-Collector Mesa Etch

Wafer Number	PB 110294
Date	12/15/94

Process	Parameters			Remarks
Preparation	Tergitol 10:1 + DI water clean			
	30 min prebake at 115° C			Oven
	Iso-Propanol rinse while spinning			
Photolith	Photoresist		4110 AZ	
	Speed		4 krpm	
	Time		40 sec	
	Prebake	Temp	100 °C	Hot Plate
		Time	2 min	
	Exposure	Power	275 W	
		time	3.0 sec	
	Developer	400 K		
		Conc.	4:1	
		Time	55 sec	
	De-Scum method		O_2 Plasma	
	RIE Machine		μ-RIE	
	Pressure		300 mtorr	
	Power		100 W	
	Time		80 sec	
	Postbake	Temp	115 °C	Oven
		Time	30 min	
Etching	Chemical	Ratio		
	50% Citric:H_2O: H_2O_2	5:5:1		
	Material	InGaAs		
	Time	2 min 30 sec		
	Total Etch Depth	0.2 μm		
Etching	Chemical	Quantity		
PR Strip	Solvent	Acetone +Iso		
	De-scum Machine	μ-RIE		same as above
		Time	4 min	

p and i-layer of p-i-n Mesa Etch

Wafer Number	PB 110294
Date	12/16/94

Process	Parameters			Remarks
Preparation	Tergitol 10:1 + DI water clean			
	30 min prebake at 115° C			Oven
	Iso-Propanol rinse while spinning			
Photolith	Photoresist		4110 AZ	
	Speed		4 krpm	
	Time		40 sec	
	Prebake	Temp	100 °C	Hot Plate
		Time	2 min	
	Exposure	Power	275 W	
		time	3.0 sec	
	Developer	400 K		
		Conc.	4:1	
		Time	80 sec	
	De-Scum method		O_2 Plasma	
	RIE Machine		μ-RIE	
	Pressure		300 mtorr	
	Power		100 W	
	Time		80 sec	
	Postbake	Temp	115 °C	Oven
		Time	30 min	
Etching	Chemical	Ratio		
	$HBr:H_2O:H_2O_2$	1:5:2 drops		
	Material	InP, InGaAs		
	Time	2 min 30 sec		
	Total Etch Depth	0.5 μm		side notches
Etching	Chemical	Quantity		
	50%Citric:$H_2O:H_2O_2$	5:5:1		
	Material	InGaAs		
	Time	11 min		
	Total Etch Depth	1.8 μm		notches etched off
PR Strip	Solvent	Acetone +Iso		
	De-scum Machine	μ-RIE		same as above
		Time	4 min	

n-layer of p-i-n Mesa Etch

Wafer Number	PB 110294
Date	12/17/94

Process	Parameters			Remarks
Preparation	Tergitol 10:1 + DI water clean			
	30 min prebake at 115° C			Oven
	Iso-Propanol rinse while spinning			
Photolith	Photoresist		4110 AZ	
	Speed		4 krpm	
	Time		40 sec	
	Prebake	Temp	100 °C	Hot Plate
		Time	2 min	
	Exposure	Power	275 W	
		time	3.2 sec	
	Developer	400 K		
		Conc.	4:1	
		Time	2 min	
	De-Scum method		O_2 Plasma	
	RIE Machine		μ-RIE	
	Pressure		300 mtorr	
	Power		100 W	
	Time		80 sec	
	Postbake	Temp	115 °C	Oven
		Time	30 min	
Etching	Chemical	Ratio		
	$HBr:H_2O:H_2O_2$	5:1:2 drops		
	Material	InP		
	Time	3 min 30 sec		
	Total Etch Depth	0.15 μm		side notches, some undercut
Etching	Chemical	Quantity		
PR Strip	Solvent	Acetone +Iso		
	De-scum Machine	μ-RIE		same as above
		Time	4 min	

Polyimide Deposition

Wafer Number	PB 110294
Date	12/19/94

Process	Parameters			Remarks
Preparation	Tergitol 10:1 +DI water clean			
	10 min prebake at 115 °C			
	Anneal	Program	NCON	
		Temp	365 °C	
		Time	90 sec	
	BOE Surface Etch	HF:H_2O	1:10	
		Time	5 min	
Polyimde	Type	285 OCG		
	Speed	0-4 rpm		
	Time	50 sec		
	Prebake	Temp	110 °C	Hot Plate
		Time	2 min	
Curing	Temperature	Time/Rate		
	30-150 °C	4 °C/min		
	150 °C	30 min		
	150-300 °C	4 °C/min		
	300 °C	30 min		
	300-240 °C	-2 °C/min		
	240 °C	2 min		
	OFF			
Etch Mask	Material	SiO_x		e^--beam evaporated
		I	7 mA	
		Rate	4 Å/sec	
		Thickness	1000 Å	
	Prebake	10 min @ 115 °C		Oven
Photolith	Photoresist	4210 AZ		
	Speed	4 krpm		
	Time	40 sec		
	Prebake	Temp.	100 °C	Hot Plate
		Time	1 min	
	Exposure	Power	275 W	

		Time	3.2 sec	
	Developer Type		400 K	
		Conc.	4: 1	
		Time	75 sec	
	Postbake	Temp.	115 °C	Oven
		Time	30 min	
Mask Etch	Equipment		Plasma-Therm	
	CF_4 Flow Rate		50 sccm	
	Pressure		100 mtorr	
	Power		100 W	
	Time		1 min 30 sec	
PR Strip	Solvent	Acetone +Iso		
Poly Etch	RIE Machine	Plasma-Therm		
	O_2 Flow Rate		50 sccm	
	Pressure		100 mtorr	
	Power		100 W	
	Time	4 min		
Strip Mask	Chemical	BOE		
	Time	4 min		

P-Type Metalization

Wafer Number	PB 110294
Date	12/23/94

Process	Parameters				Remarks
Cleaning	Tergiton 10:1 +DI water clean				
	10 min prebake at 115 °C				Oven
	Iso-Propanol rinse while spinning				
Photolith	Photoresist		4210 AZ		
	Speed		4 krpm		
	Time		40 sec		
	Prebake	Temp	100 °C		Hot Plate
		Time	1 min		
	Toluene Soak	Time	5 min		
	Exposure	Power	275 W		
		Time	3.2 sec		
	Developer		400 K		
		Conc.	4: 1		
		Time	2 min		
	Acid Dip	H_2SO_4	1:6		
		Time	10 sec		
Deposition	Equipment		e^--beam		rotation on
	Pressure		$6x10^{-6}$ torr		
	Metal	Pwr/I	Rate Å/s	Thick Å	
	Ti	54 mA	3.6	500	
	Pt	137 mA	3.8	500	
	Au	65 mA	4.4	1000	
	Final Temp		55 °C		
Lift-Off	Solvent		Aceton +Iso		OK

N-Type Metalization

Wafer Number	PB 110294
Date	12/24/94

Process	Parameters				Remarks
Cleaning	Tergiton 10:1 +DI water clean				
	10 min prebake at 115 °C				Oven
	Iso-Propanol rinse while spinning				
Photolith	Photoresist		4210 AZ		
	Speed		4 krpm		
	Time		40 sec		
	Prebake	Temp	100 °C		Hot Plate
		Time	1 min		
	Toluene Soak	Time	5 min		
	Exposure	Power	275 W		
		Time	3.4 sec		
	Developer		400 K		
		Conc.	4: 1		
		Time	2.5 min		
	Acid Dip	H_2SO_4	1:6		
		Time	10 sec		
Deposition	Equipment	e^--beam			rotation on
	Pressure	$5x10^{-6}$ torr			
	Metal	Pwr/I	Rate Å/s	Thick Å	
	Ge	29 mA	3.5	270	
	Au	66 mA	3.4	450	
	Ni	33 mA	2.3	215	
	Au	64 mA	3.2	1000	
	Final Temp		45 °C		
Lift-Off	Solvent	Aceton +Iso			OK

Ti-Resistor Metalization

Wafer Number	PB 110294
Date	12/23/94

Process	Parameters				Remarks
Cleaning	Tergiton 10:1 +DI water clean				
	10 min prebake at 115 °C				Oven
	Iso-Propanol rinse while spinning				
Photolith	Photoresist		4210 AZ		
	Speed		4 krpm		
	Time		40 sec		
	Prebake	Temp	100 °C		Hot Plate
		Time	1 min		
	Toluene Soak	Time	5 min		
	Exposure	Power	275 W		
		Time	3.2 sec		
	Developer		400 K		
		Conc.	4: 1		
		Time	75 sec		
Deposition	Equipment		e^--beam		rotation on
	Pressure		$6x10^{-6}$ torr		
	Metal	Pwr/I	Rate	Thick	
	Ti	70 mA	3.4 Å/s	2500 Å	
	Final Temp		65 °C		
Lift-Off	Solvent		Aceton +Iso		OK

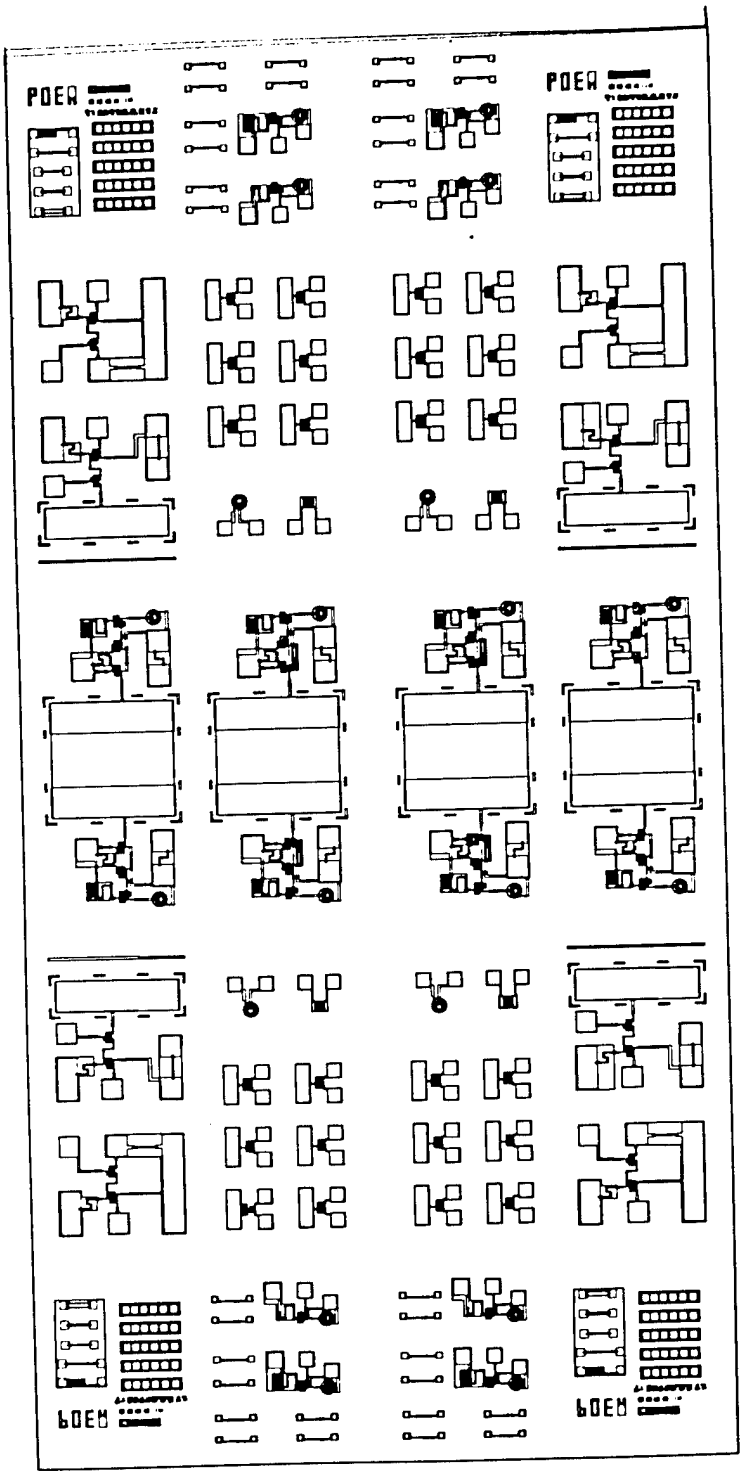
Interconnect/Pad Metalization

Wafer Number	PB 110294
Date	12/27/94

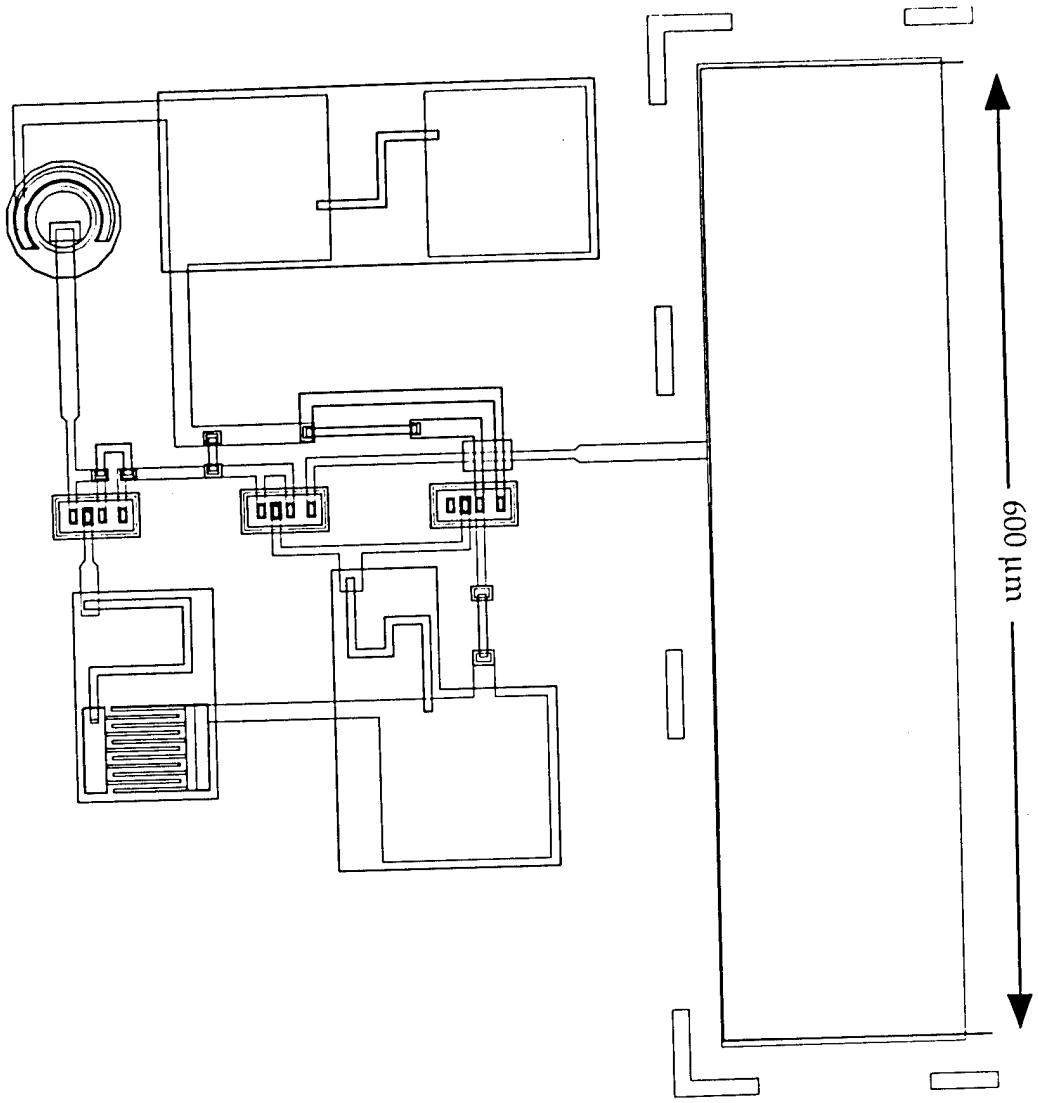
Process	Parameters				Remarks
Cleaning	Tergiton 10:1 +DI water clean				
	10 min prebake at 115 °C				Oven
	Iso-Propanol rinse while spinning				
Photolith	Photoresist		4210 AZ		
	Speed		4 krpm		
	Time		40 sec		
	Prebake	Temp	100 °C		Hot Plate
		Time	1.5 min		
**Double	Flood Exposure	Power	275 W		
**Layer		Time	20 sec		
	Photoresist		4210 AZ		
	Speed		4 krpm		
	Time		40 sec		
	Prebake	Temp	100 °C		Hot Plate
		Time	1.5 min		
	Toluene		5 min		
	Exposure	Power	275 W		
		Time	3.3 sec		
	Developer		400 K		
		Conc.	3.5: 1		
		Time	1 min		
	Acid Dip		----		
		Time	----		
Deposition	Equipment		e^--beam		
	Pressure		$5x10^{-6}$ torr		rotation on
	Metal	Pwr/I	Rate Å/s	Thick Å	
	Ti	76 mA	2.8	200	
	Au	85 mA	2.0	10,000	
	Final Temp		76 °C		

Appendix D

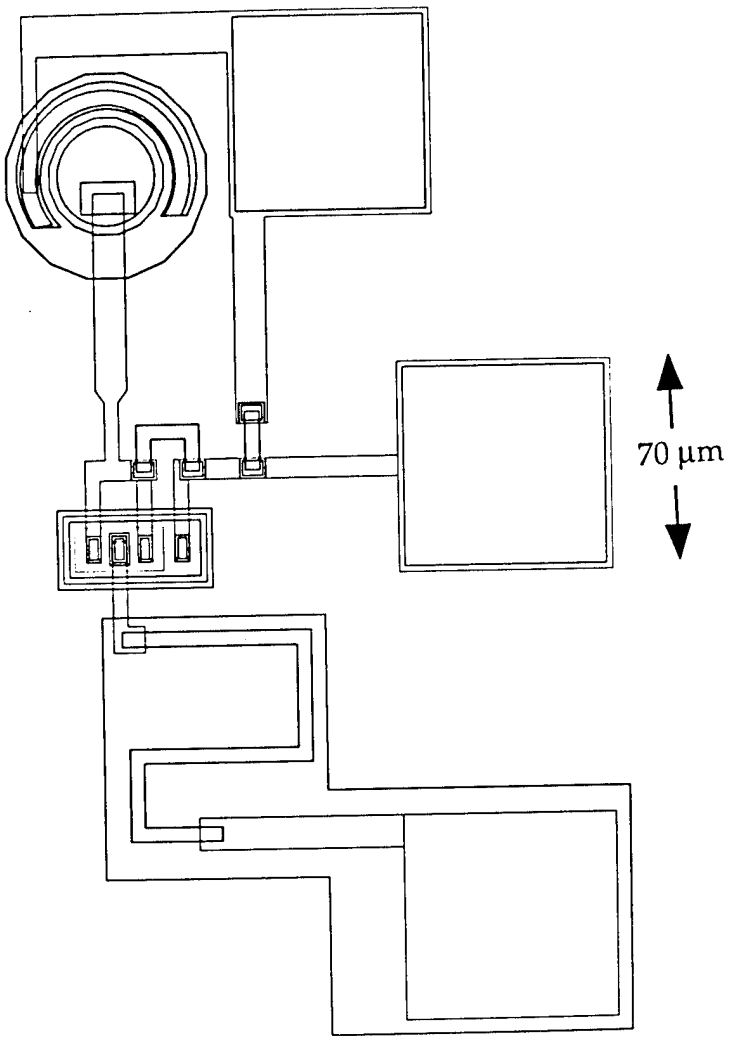
Mask Layout for the Smart Pixel



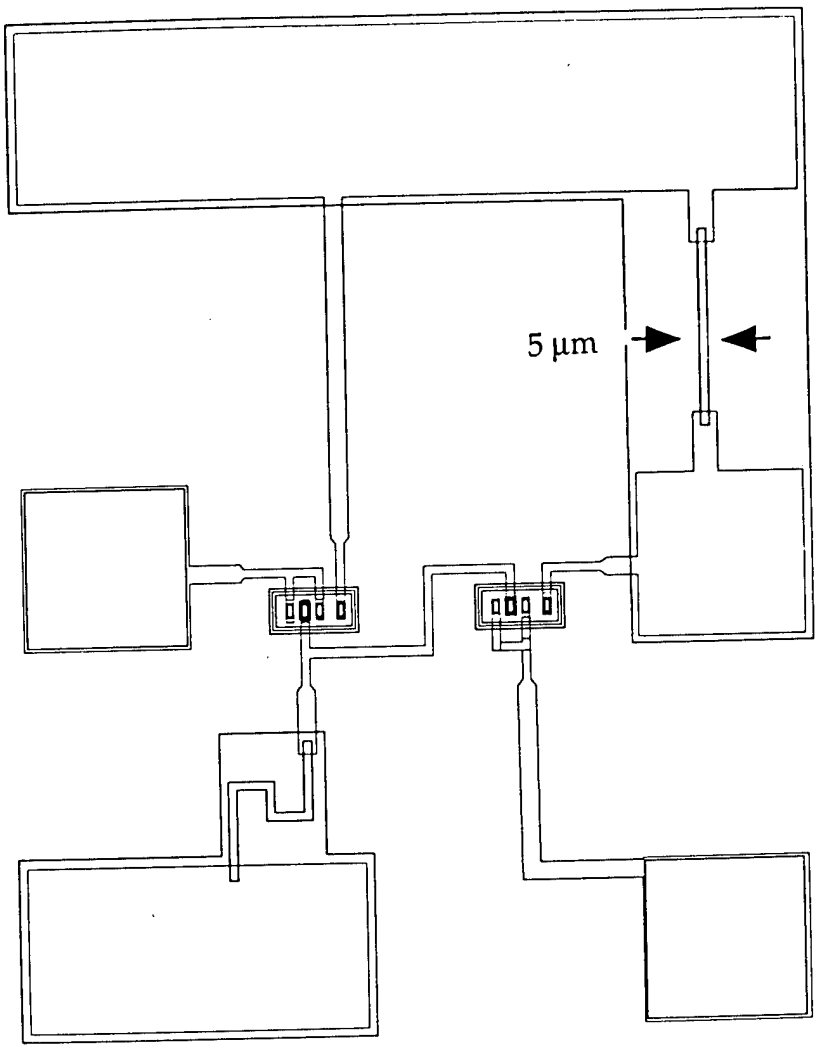
D.1: Composite drawing of the smart pixel module.



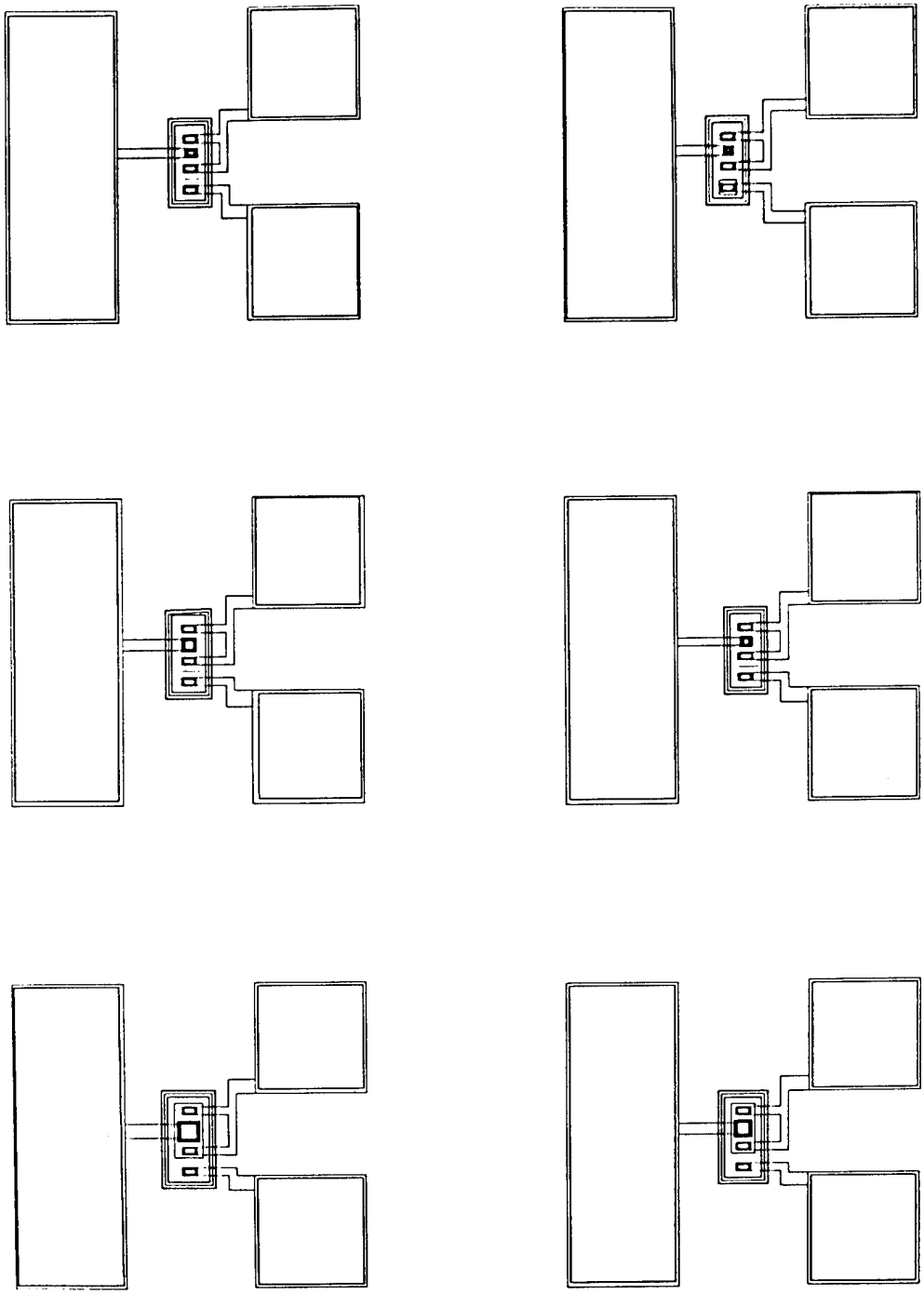
D.2: The smart pixel circuit layout.



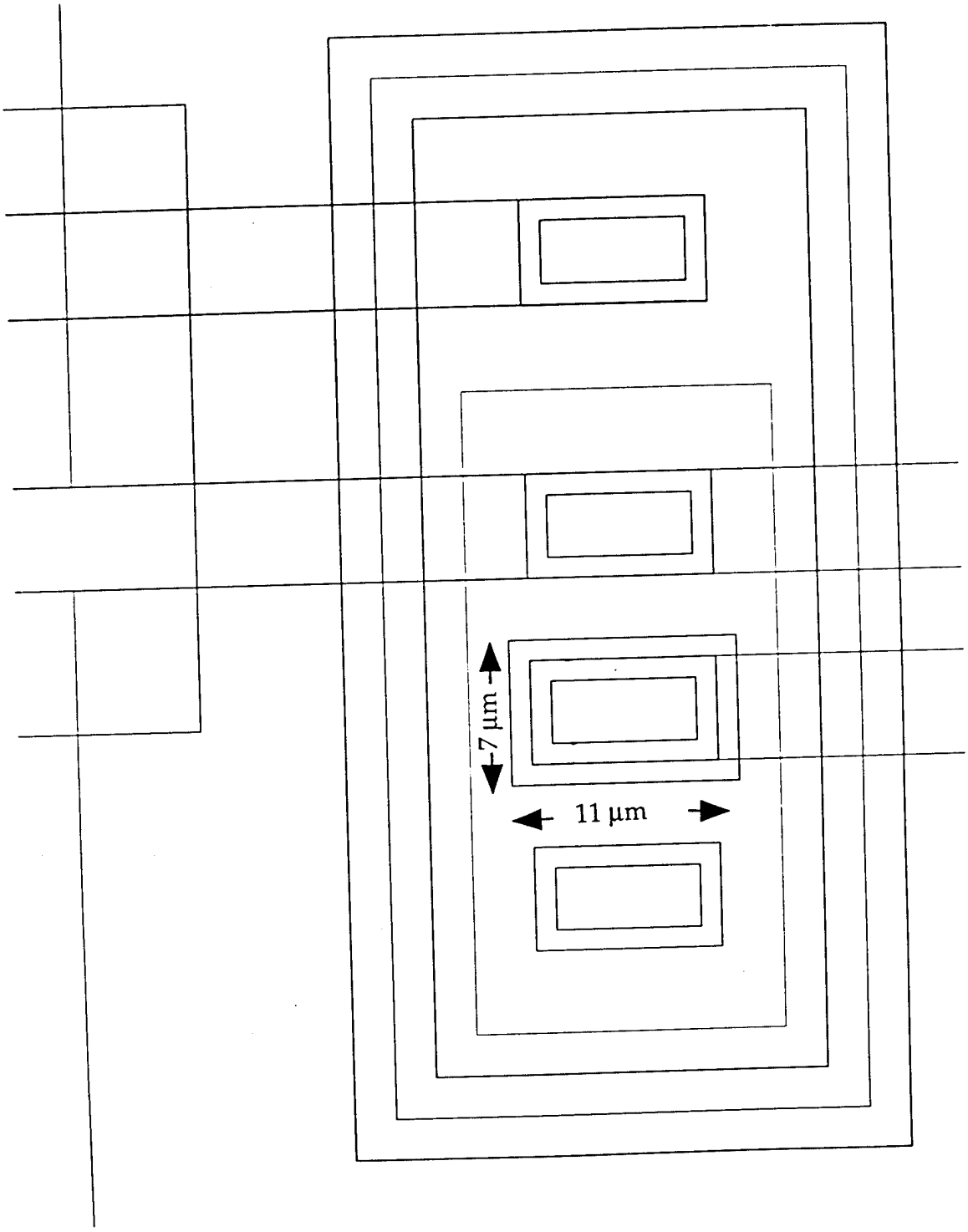
D.3: The front end test circuit.



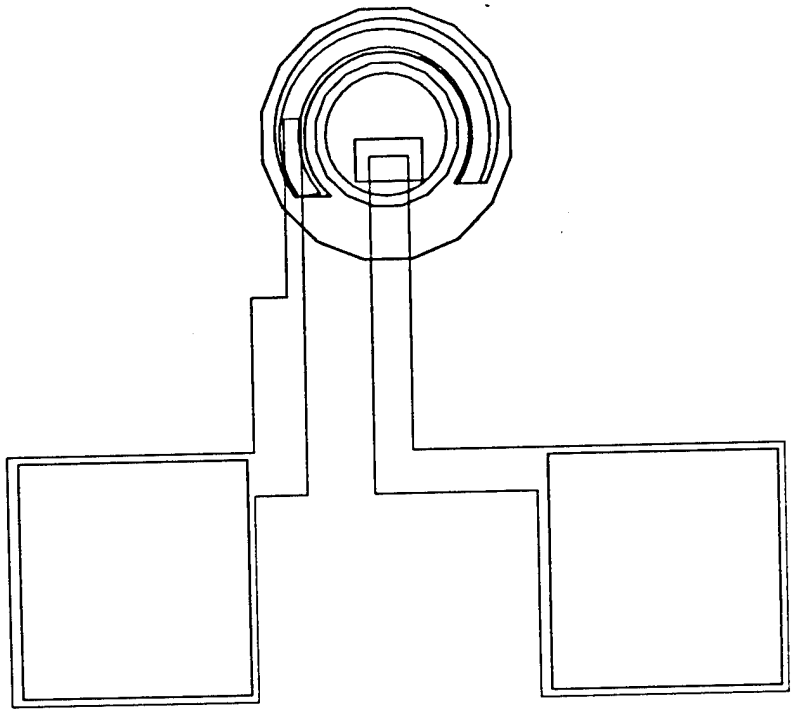
D.4: The differential pair test circuit.



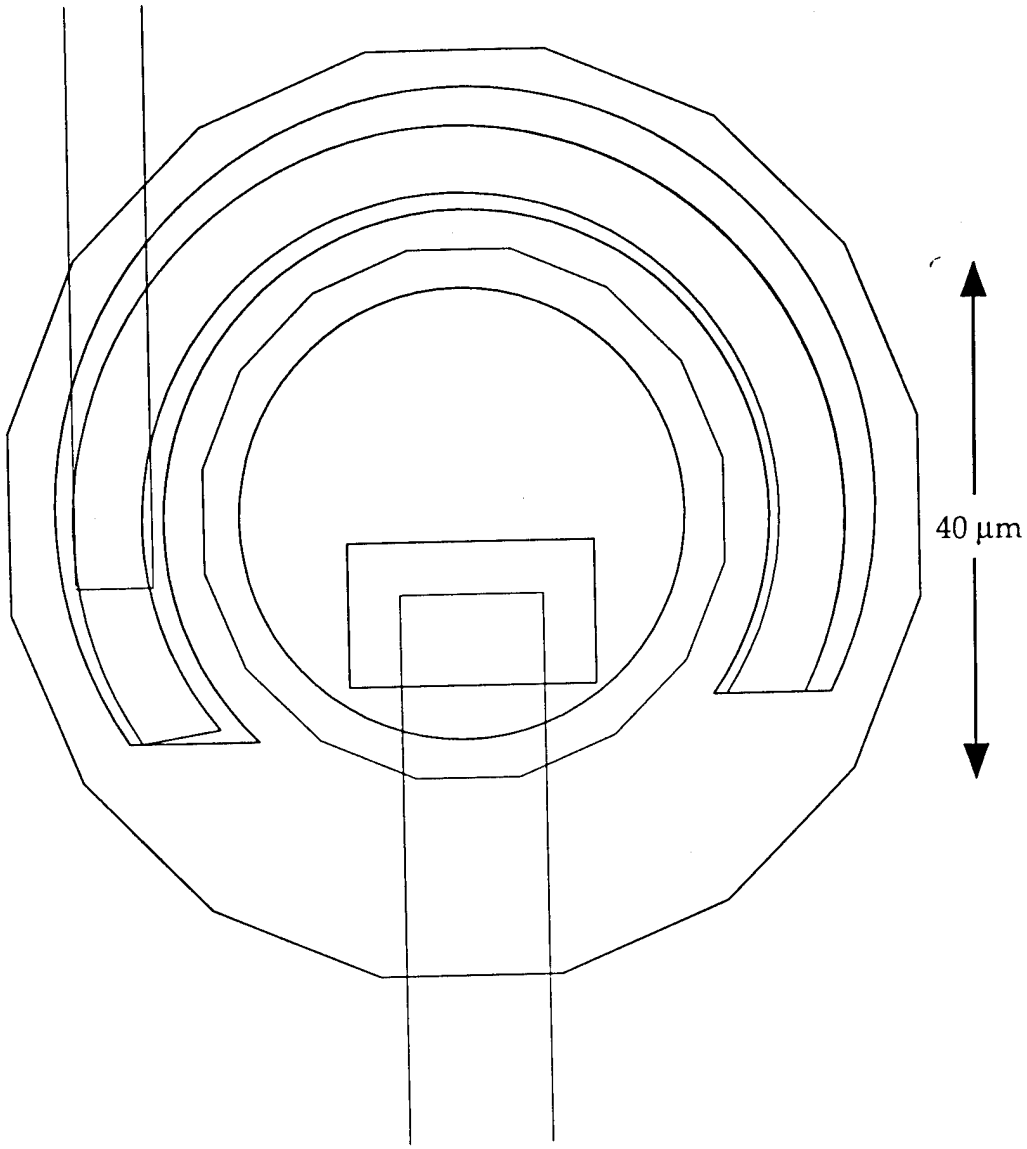
D.5: Test HBT units with different emitter areas.



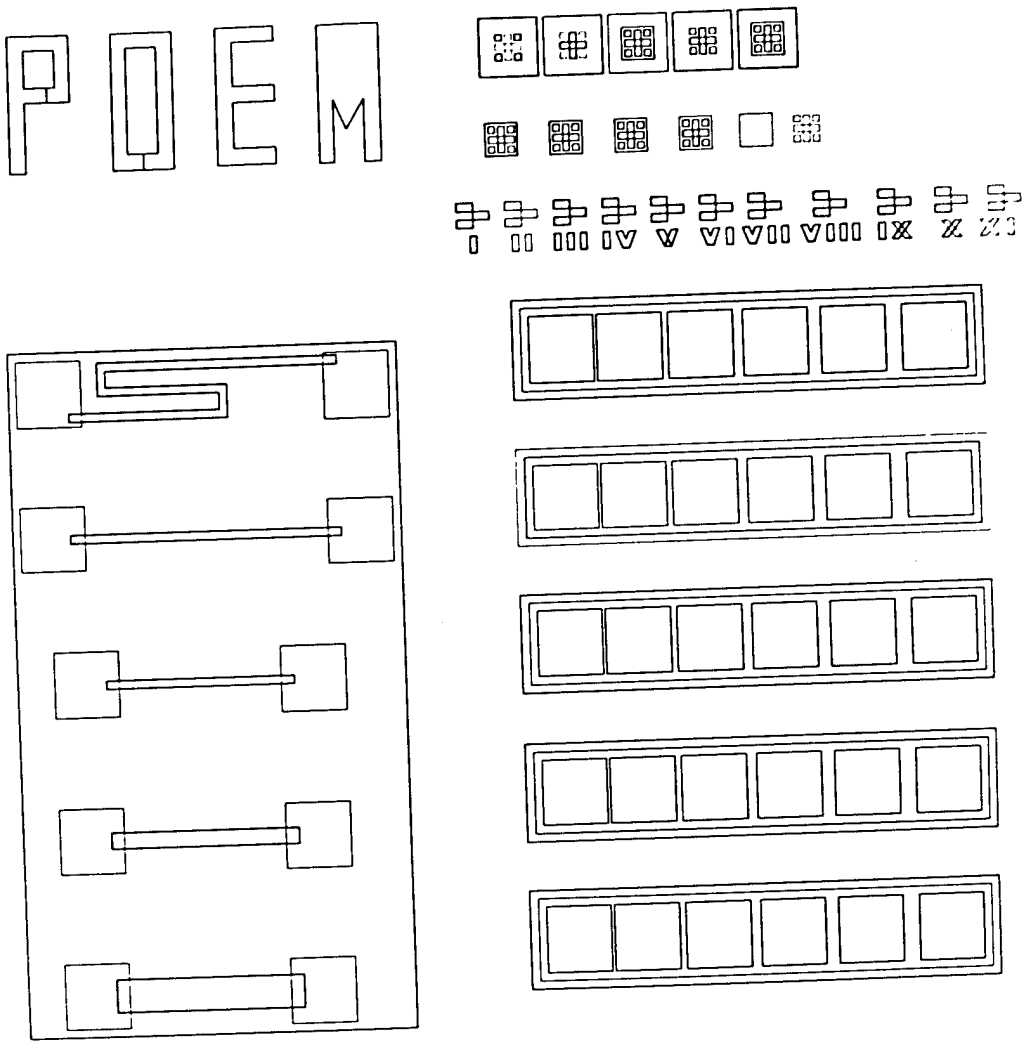
D.6: The close-up view of an HBT mask layout.



D.7: The p-i-n photodiode test unit.



D.8: Close-up view of the p-i-n mesa.



D.9: The alignment marks, TLM patterns for contact resistance characterization, and metal think film resistor test units.